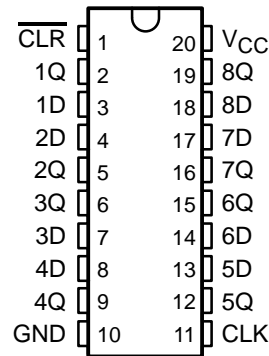


# SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

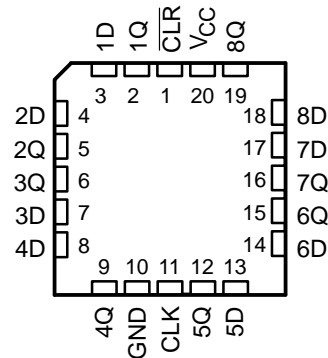
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVTH273 . . . J PACKAGE  
SN74LVTH273 . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LVTH273 . . . FK PACKAGE  
(TOP VIEW)



## description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH273 are positive-edge-triggered flip-flops with a direct clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVTH273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed circuit board area.

The SN54LVTH273 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LVTH273 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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**TEXAS  
INSTRUMENTS**

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# SN54LVTH273, SN74LVTH273

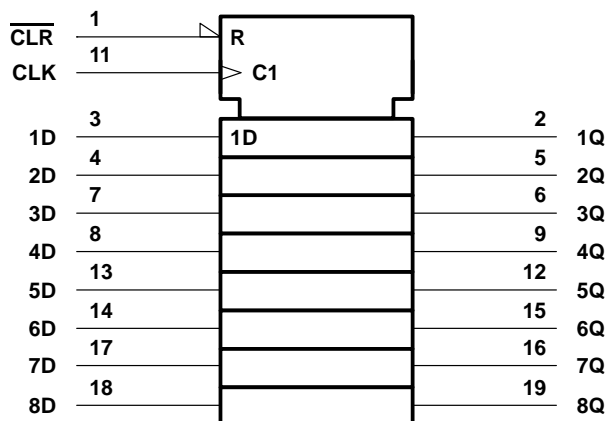
## 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136F – MAY 1992 – REVISED DECEMBER 1996

FUNCTION TABLE  
(each flip-flop)

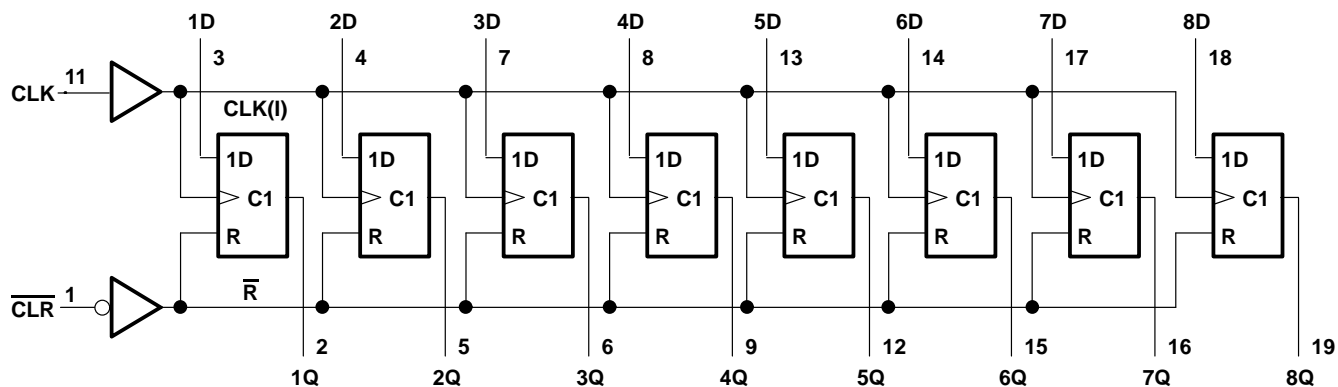
INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	H or L	X	$Q_0$

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



# SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136F – MAY 1992 – REVISED DECEMBER 1996

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVTH273	96 mA
SN74LVTH273	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH273	48 mA
SN74LVTH273	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

## recommended operating conditions (see Note 4)

		SN54LVTH273		SN74LVTH273		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

# SN54LVTH273, SN74LVTH273

## 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS

### WITH CLEAR

SCBS136F – MAY 1992 – REVISED DECEMBER 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54LVTH273			SN74LVTH273			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$				-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2						
		$I_{OH} = -32\text{ mA}$				2			
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4			0.4	
		$I_{OL} = 32\text{ mA}$			0.5			0.5	
		$I_{OL} = 48\text{ mA}$			0.55				
		$I_{OL} = 64\text{ mA}$						0.55	
$I_I$	$V_{CC} = 0\text{ or } 3.6\text{ V}$ , $V_I = 5.5\text{ V}$				10			10	$\mu\text{A}$
	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}\text{ or GND}$	Control inputs		$\pm 1$			$\pm 1$	
		$V_I = V_{CC}$	Data inputs		1			1	
		$V_I = 0$			-5			-5	
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$				$\pm 100$			$\pm 100$	$\mu\text{A}$
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	Data inputs		75			75	$\mu\text{A}$
		$V_I = 2\text{ V}$			-75			-75	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$	$I_O = 0$	Outputs high		0.19			0.19	mA
			Outputs low		5			5	
$\Delta I_{CC}^\ddagger$	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$				0.2			0.2	mA
$C_i$	$V_I = 3\text{ V or } 0$				4			4	pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		SN54LVTH273				SN74LVTH273				UNIT
		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	150			0	150			MHz
$t_w$	Pulse duration	3.3		3.3		3.3		3.3		ns
$t_{su}$	Setup time, data high or low before CLK↑	2.3		2.7		2.3		2.7		ns
	Setup time, $\overline{\text{CLR}}$ high before CLK↑	2.3		2.7		2.3		2.7		
$t_h$	Hold time, data high or low after CLK↑	0		0		0		0		ns

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# SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136F – MAY 1992 – REVISED DECEMBER 1996

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH273				SN74LVTH273				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f <sub>max</sub>			150				150					MHz
t <sub>PLH</sub>	CLK	Any Q	1.6	5	5.6		1.7	3.2	4.9	5.5		ns
t <sub>PHL</sub>			1.8	4.9	5.2		1.9	3.2	4.8	5.1		
t <sub>PHL</sub>	CLR	Any Q	1.5	4.4	4.8		1.6	2.7	4.3	4.7		ns

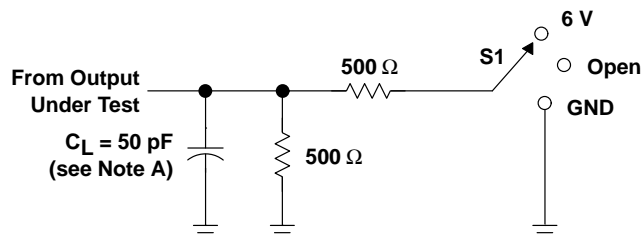
† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# SN54LVTH273, SN74LVTH273

## 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

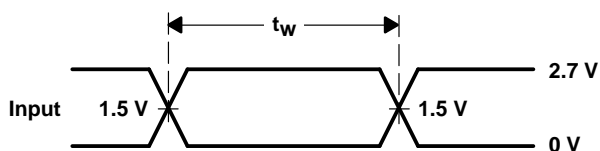
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### PARAMETER MEASUREMENT INFORMATION

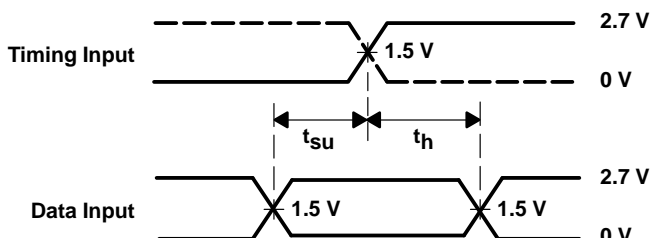


LOAD CIRCUIT

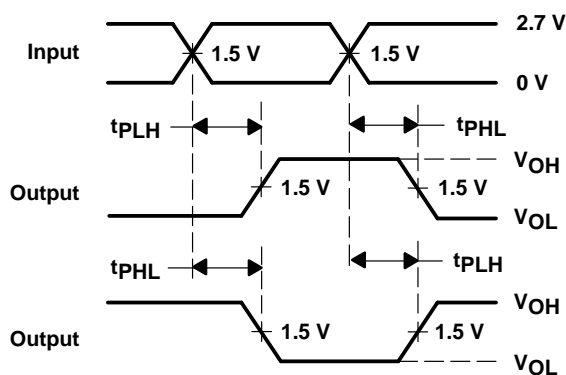
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



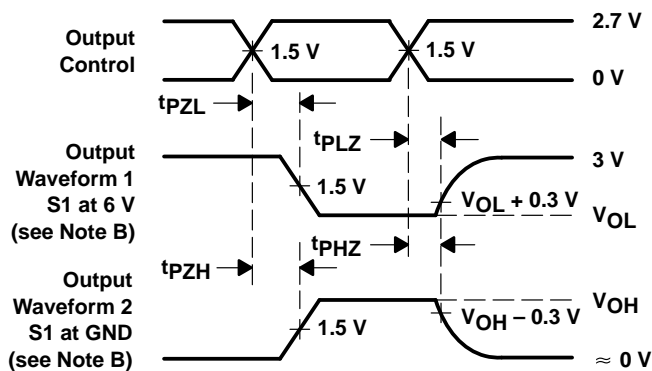
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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