- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **64 × 36 Clocked FIFO Buffering Data From Port A to Port B**
- **Mailbox-Bypass Register In Each Direction**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **Full Flag ($\overline{FF}$) and Almost-Full Flag ($\overline{AF}$) Synchronized by CLKA**
- **Empty Flag ($\overline{EF}$) and Almost-Empty Flag ($\overline{AE}$) Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat (PCB) and 132-Pin Plastic Quad Flat (PQ) Packages**

description

The SN74ABT3611 is a high-speed, low-power BiCMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. A 64 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words are stored in memory. Communication between each port can take place through two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider datapaths.

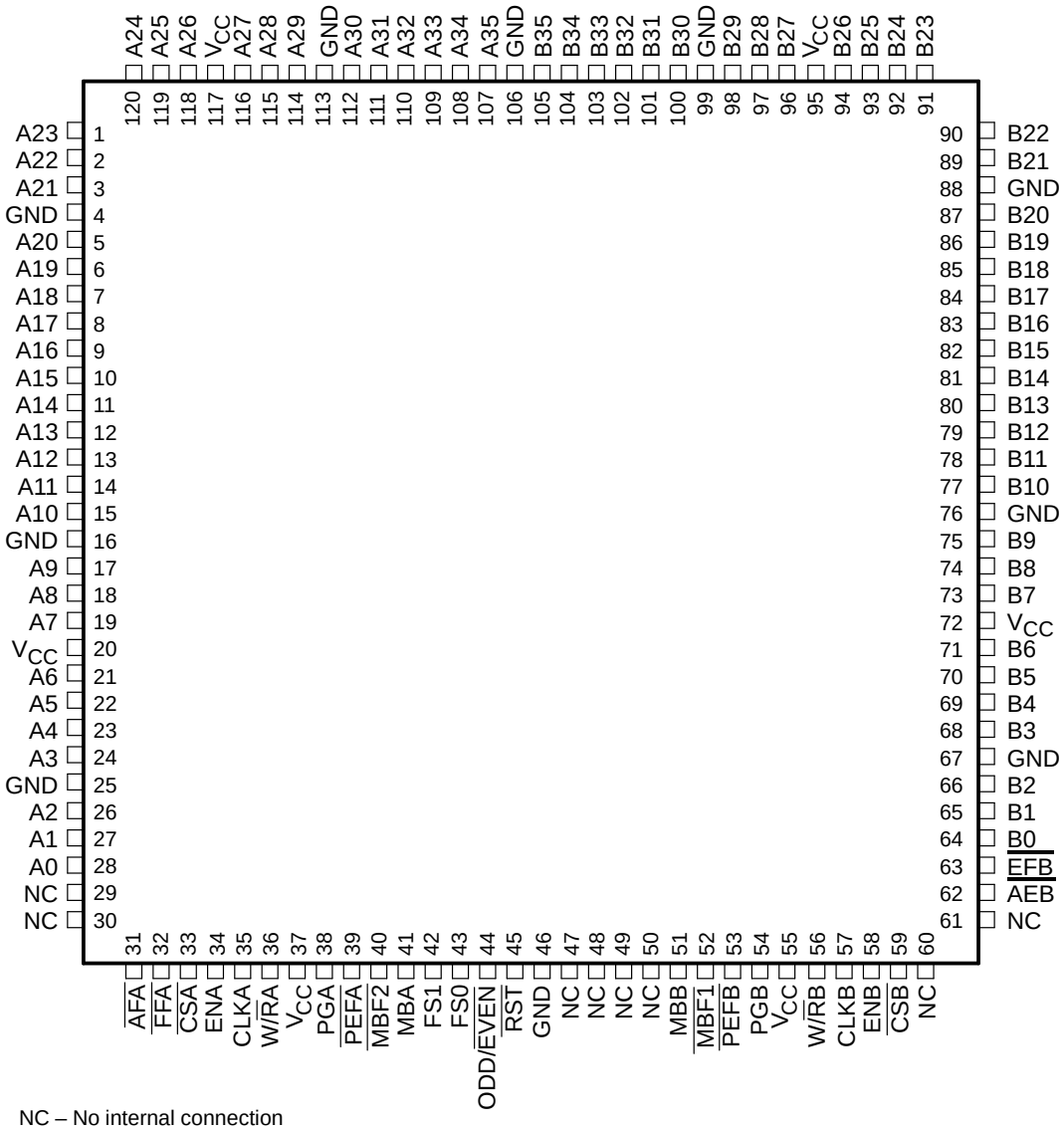
The SN74ABT3611 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The full flag ($\overline{FF}$) and almost-full flag ($\overline{AF}$) of the FIFO are two-stage synchronized to the port clock that writes data to its array (CLKA). The empty flag ($\overline{EF}$) and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to the port clock that reads data from array (CLKB).

The SN74ABT3611 is characterized for operation from 0°C to 70°C.

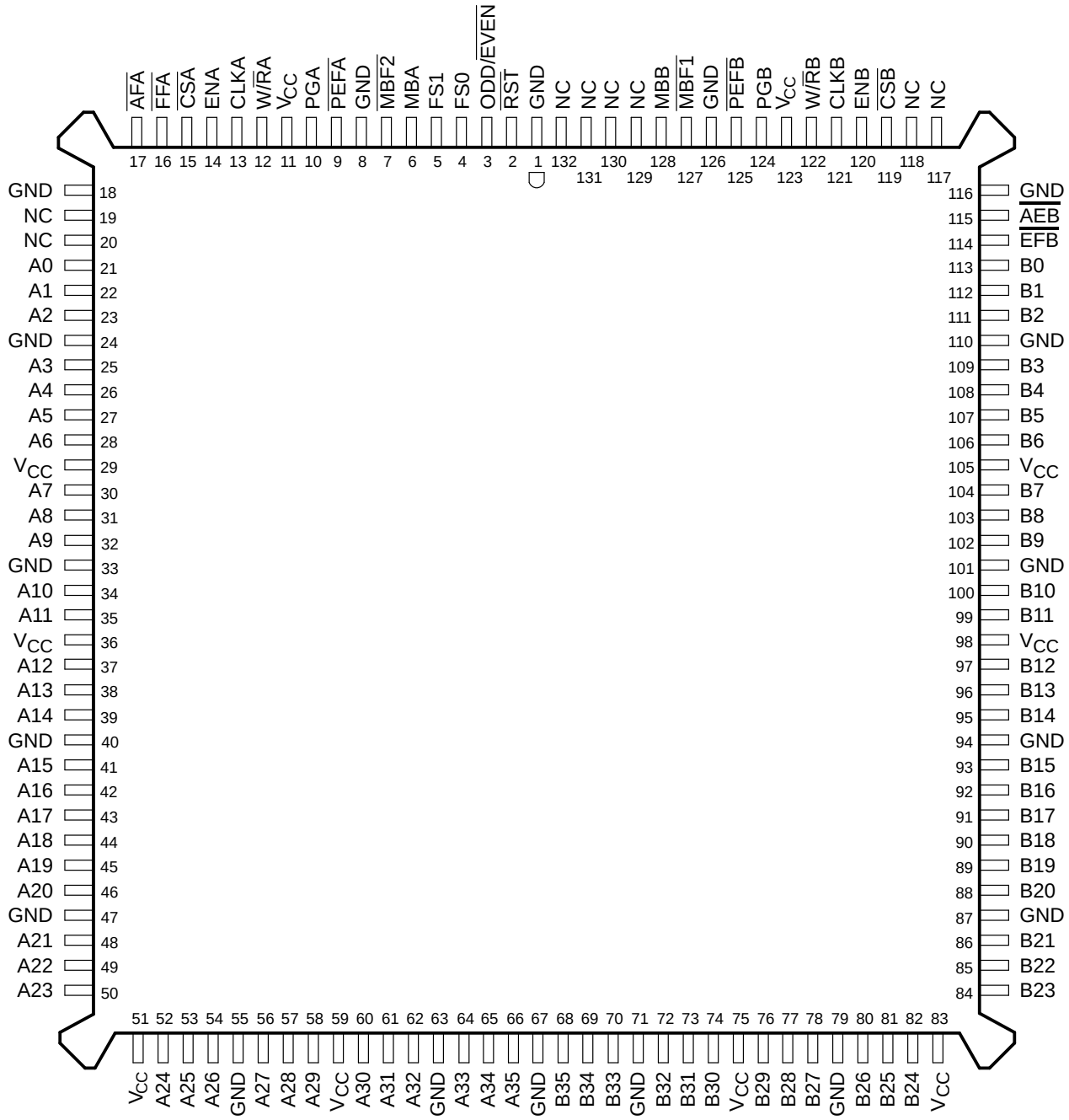
For more information on this device family, see the application reports *FIFO Mailbox-Bypass Registers: Using Bypass Registers to Initialize DMA Control* and *Parity-Generate and Parity-Check Features for High-Bandwidth-Computing FIFO Applications* in the 1996 *High-Performance FIFO Memories Designer's Handbook*, literature number SCAA012A.

PCB PACKAGE
(TOP VIEW)



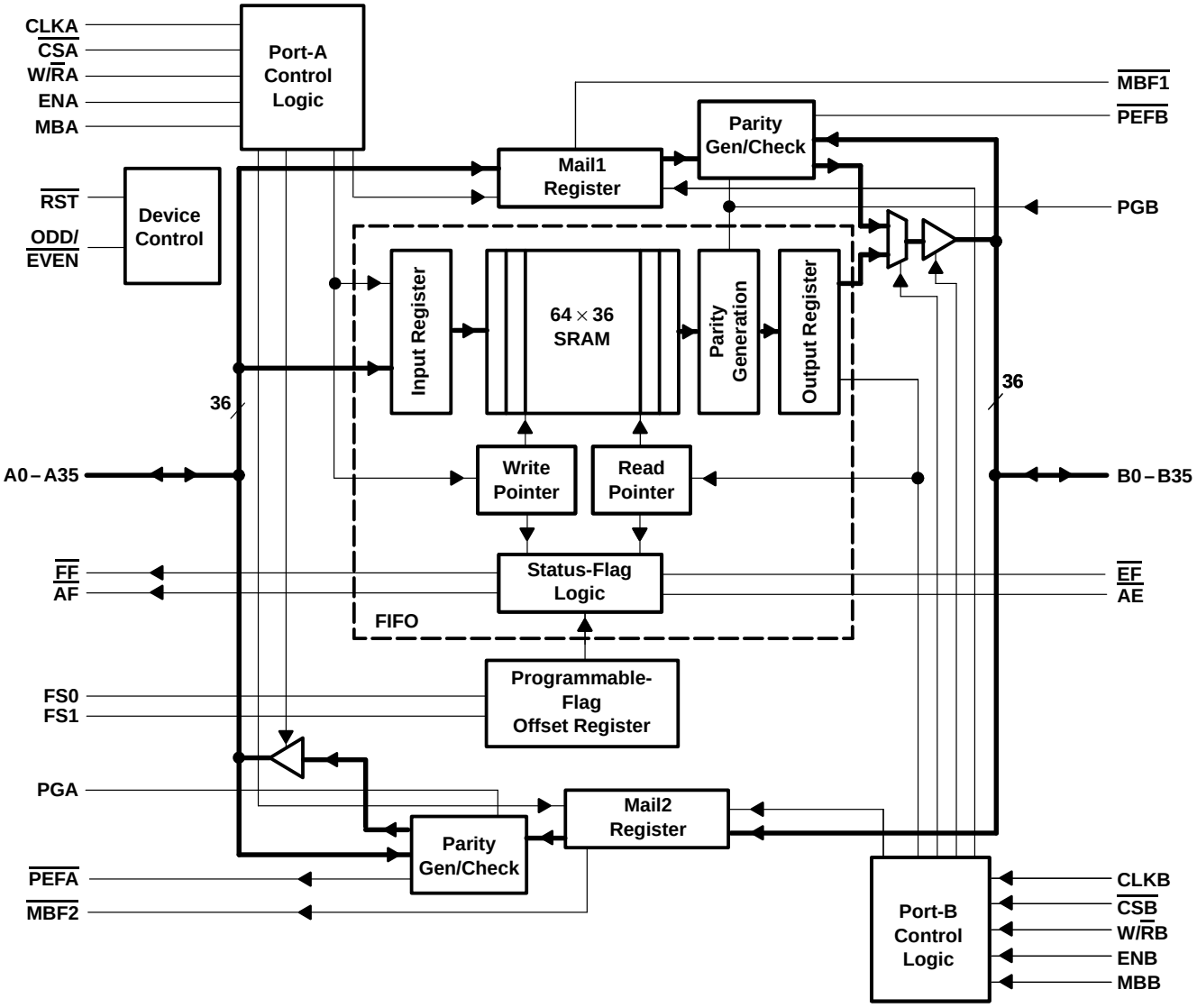
NC – No internal connection

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

functional block diagram



TEXAS INSTRUMENTS
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Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AE}$	O	Almost-empty flag. Programmable flag synchronized to CLKB. $\overline{AE}$ is low when the number of words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	O	Almost-full flag. Programmable flag synchronized to CLKA. $\overline{AF}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
$\overline{EF}$	O	Empty flag. $\overline{EF}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EF}$ is low, the FIFO is empty and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{EF}$ is high. $\overline{EF}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{FF}$	O	Full flag. $\overline{FF}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FF}$ is low, the FIFO is full and writes to its memory are disabled. $\overline{FF}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
FS1, FS0	I	Flag-offset selects. The low-to-high transition of $\overline{RST}$ latches the values of FS0 and FS1, which loads one of four preset values into the almost-full and almost-empty offset register, X.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects the FIFO output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high when the device is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high when the device is reset.
ODD/$\overline{EVEN}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{EVEN}$ is high and even parity is checked when ODD/$\overline{EVEN}$ is low. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	O (port A)	Port-A parity error flag. When any byte applied to A0–A35 fails parity, $\overline{PEFA}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of ODD/$\overline{EVEN}$. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is set up by having $\overline{CSA}$ low, ENA high, W/$\overline{RA}$ low, MBA high, and PGA high, $\overline{PEFA}$ is forced high regardless of the state of the A0–A35 inputs.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
$\overline{\text{PEFB}}$	O (port B)	Port-B parity error flag. When any byte applied to terminals B0–B35 fails parity, $\overline{\text{PEFB}}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of ODD/$\overline{\text{EVEN}}$. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is set up by having $\overline{\text{CSB}}$ low, ENB high, W/$\overline{\text{R}}$B low, MBB high, and PGB high, $\overline{\text{PEFB}}$ is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for mail2 register reads from port A when PGA is high. The type of parity generated is selected by the state of ODD/$\overline{\text{EVEN}}$. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of ODD/$\overline{\text{EVEN}}$. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. This sets $\overline{\text{AF}}$, $\overline{\text{MBF1}}$, and $\overline{\text{MBF2}}$ high and $\overline{\text{EF}}$, $\overline{\text{AE}}$, and $\overline{\text{FF}}$ low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of FS1 and FS0 to select $\overline{\text{AF}}$ and $\overline{\text{AE}}$ flag offset.
W/$\overline{\text{R}}$A	I	Port-A write/read select. W/$\overline{\text{R}}$A high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{R}}$A is high.
W/$\overline{\text{R}}$B	I	Port-B write/read select. W/$\overline{\text{R}}$B high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{\text{R}}$B is high.

detailed description

reset

The SN74ABT3611 is reset by taking the reset ($\overline{\text{RST}}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. $\overline{\text{RST}}$ can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the full flag ($\overline{\text{FF}}$) low, the empty flag ($\overline{\text{EF}}$) low, the almost-empty flag ($\overline{\text{AE}}$) low, and the almost-full flag ($\overline{\text{AF}}$) high. A reset also forces the mailbox flags ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) high. After a reset, $\overline{\text{FF}}$ is set high after two low-to-high transitions of CLKA. The device must be reset after power up before data is written to its memory.

A low-to-high transition on $\overline{\text{RST}}$ loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{R}}$A). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{R}}$A is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{R}}$A are low. Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is high, ENA is high, MBA is low, and $\overline{\text{FF}}$ is high (see Table 2).

FIFO write/read operation (continued)

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{R}$A	ENA	MBA	CLKA	A0 – A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

The port-B control signals are identical to those of port A. The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{R}$B). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{R}$B is high. The B0–B35 outputs are active when both $\overline{CSB}$ and W/$\overline{R}$B are low. Data is read from the FIFO to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{R}$B is low, ENB is high, MBB is high, and $\overline{EF}$ is high (see Table 3).

Table 3. Port-B Enable Function Table

$\overline{CSB}$	W/$\overline{R}$B	ENB	MBB	CLKB	B0 – B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	None
L	H	H	H	↑	In high-impedance state	Mail2 write
L	L	L	L	X	Active, FIFO output register	None
L	L	H	L	↑	Active, FIFO output register	FIFO read
L	L	L	H	X	Active, mail1 register	None
L	L	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup- and hold-time constraints to the port clocks for the port-chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{R}$A, W/$\overline{R}$B) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port-chip select and write/read select can change states during the setup- and hold-time window of the cycle.

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1996 *High-Performance FIFO Memories Data Book,* literature number SCAD003C). $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of the flags to the FIFO.

Table 4. FIFO Flag Operation

NUMBER OF WORDS IN THE FIFO	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flag ($\overline{EF}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array (CLKB). When $\overline{EF}$ is high, new data can be read to the FIFO output register. When $\overline{EF}$ is low, the FIFO is empty and attempted FIFO reads are ignored.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls $\overline{EF}$ monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles; therefore, $\overline{EF}$ is low if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1}, or greater, after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 4).

full flag ($\overline{FF}$)

The FIFO full flag is synchronized to the port clock that writes data to its array (CLKA). When $\overline{FF}$ is high, an SRAM location is free to receive new data. No memory locations are free when $\overline{FF}$ is low and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write pointer is incremented. The state machine that controls $\overline{FF}$ monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three port-A clock cycles. $\overline{FF}$ is low if less than two CLKA cycles have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets $\overline{FF}$ high and data can be written in the following clock cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1}, or greater, after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 5).

almost-empty flag ($\overline{AE}$)

The FIFO almost-empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls $\overline{AE}$ monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). $\overline{AE}$ is low when the FIFO contains X or less words in memory and is high when the FIFO contains (X + 1) or more words.

Two low-to-high transitions on the port-B clock (CLKB) are required after a FIFO write for the almost-empty flag to reflect the new level of fill. The almost-empty flag ($\overline{AE}$) of a FIFO containing (X + 1) or more words remains low if two CLKB cycles have not elapsed since the write that filled the memory to the (X + 1) level. $\overline{AE}$ is set high by the second CLKB low-to-high transition after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition on CLKB begins the first synchronization cycle if it occurs at time t_{sk2}, or greater, after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

almost-full flag ($\overline{AF}$)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls $\overline{AF}$ monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). $\overline{AF}$ is low when the FIFO contains (64 – X) or more words in memory and is high when the FIFO contains [64 – (X + 1)] or less words.

Two low-to-high transitions on the port-A clock (CLKA) are required after a FIFO read for $\overline{AF}$ to reflect the new level of fill. The almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two CLKA cycles have not elapsed since the read that reduced the number of words in memory to [64 – (X + 1)]. $\overline{AF}$ is set high by the second CLKA low-to-high transition after the FIFO read that reduces the number of words in memory to [64 – (X + 1)]. A low-to-high transition on CLKA begins the first synchronization cycle if it occurs at time t_{sk2}, or greater, after the read that reduces the number of words in memory to [64 – (X + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

mailbox registers

Two 36-bit bypass registers are on the SN74ABT3611 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port-data-transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by($\overline{CSA}$, W/$\overline{RA}$, and ENA) with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by ($\overline{CSB}$, W/$\overline{RB}$, and ENB) with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when MBB is low and from the mail1 register when MBB is high. Mail2 data is always present on A0–A35 outputs when they are active. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

parity checking

The port-A (A0–A35) inputs and port-B (B0–B35) inputs each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a low level on the port-parity-error flag ($\overline{PEFA}$, $\overline{PEFB}$). Odd or even parity checking can be selected and the parity-error flags can be ignored if this feature is not desired.

parity checking (continued)

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\text{EVEN}}$) select input. A parity error on one or more bytes of a port is reported by a low level on the corresponding port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, and port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35. When odd/even parity is selected, $\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$ is low if any byte on the port has an odd/even number of low levels applied to its bits.

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{\text{CSA}}$ low, ENA high, W/$\overline{\text{RA}}$ low, MBA high, and PGA high, $\overline{\text{PEFA}}$ is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{\text{CSB}}$ low, ENB high, W/$\overline{\text{RB}}$ low, MBB high, and PGB high, $\overline{\text{PEFB}}$ is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity-generate select (PGA) or port-B parity-generate select (PGB) enables the SN74ABT3611 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all 36 inputs regardless of the state of the parity-generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\text{EVEN}}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-B parity generate select (PGB) and ODD/$\overline{\text{EVEN}}$ have setup- and hold-time constraints to the port-B clock (CLKB) for a rising edge of CLKB used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$ is low, MBA, MBB is high, $\overline{\text{CSA}}$, $\overline{\text{CSB}}$ is low, ENA, ENB is high, and PGA, PGB is high. Generating parity for mail-register data does not change the contents of the register.

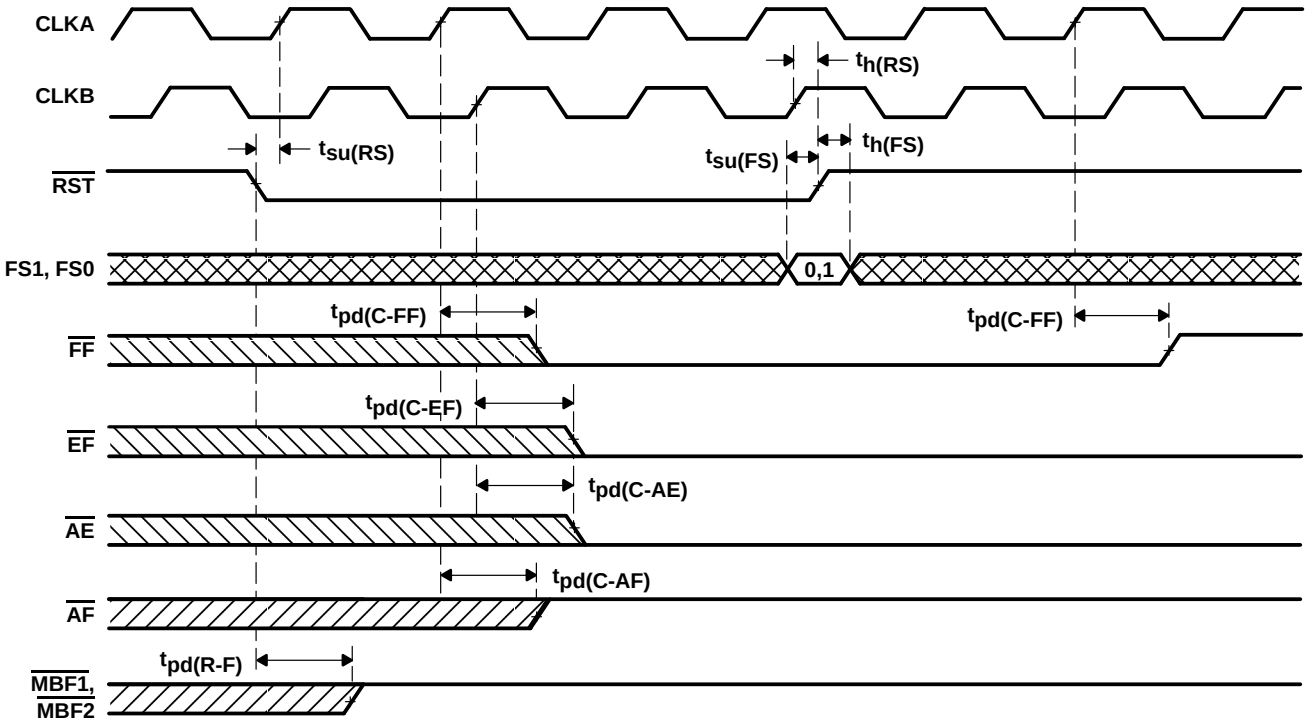


Figure 1. Device Reset Loading the X Register With the Value of Eight

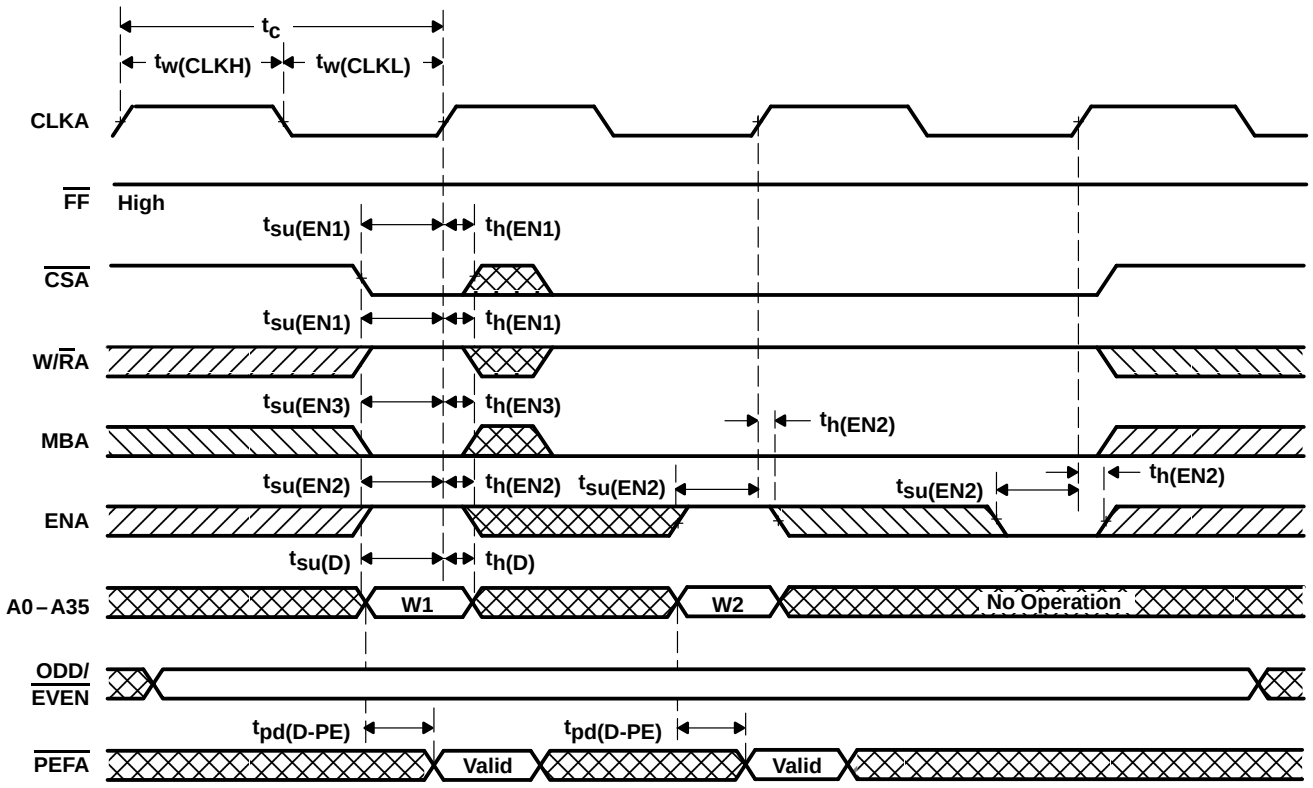


Figure 2. FIFO1-Write-Cycle Timing

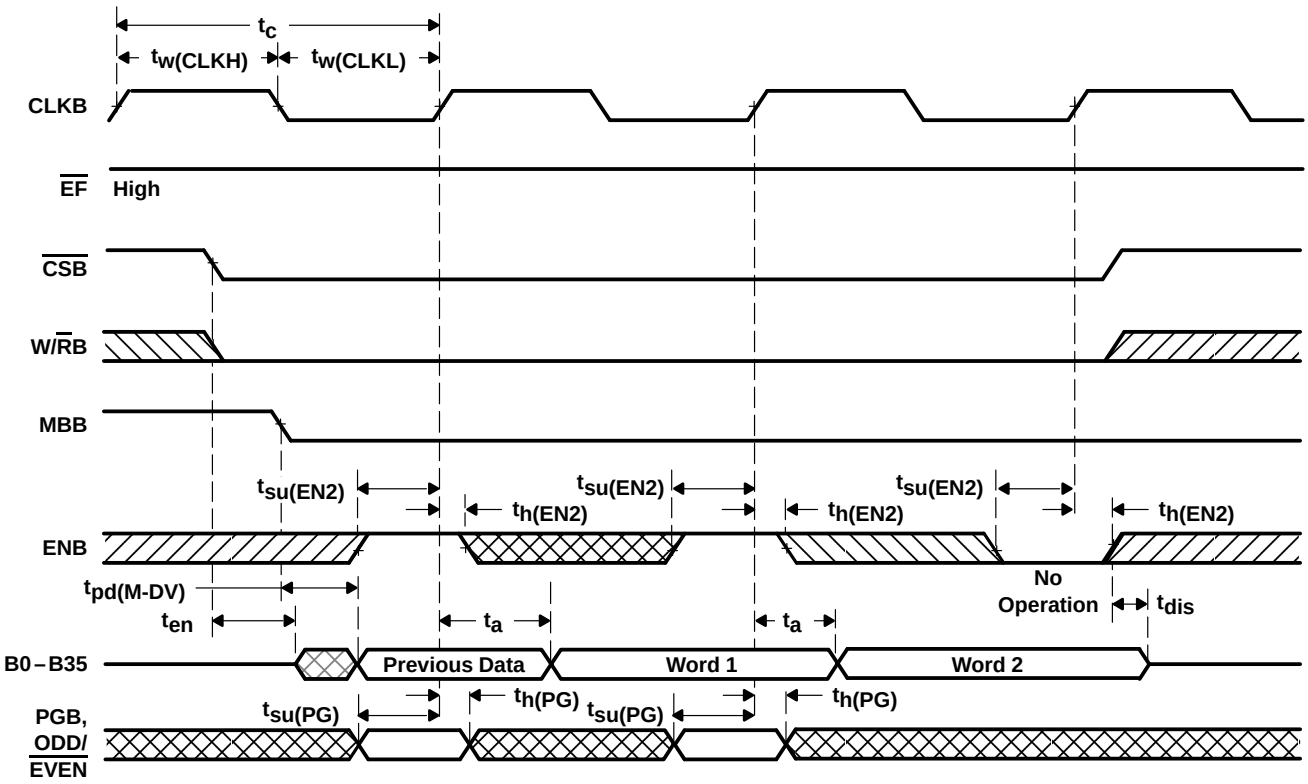
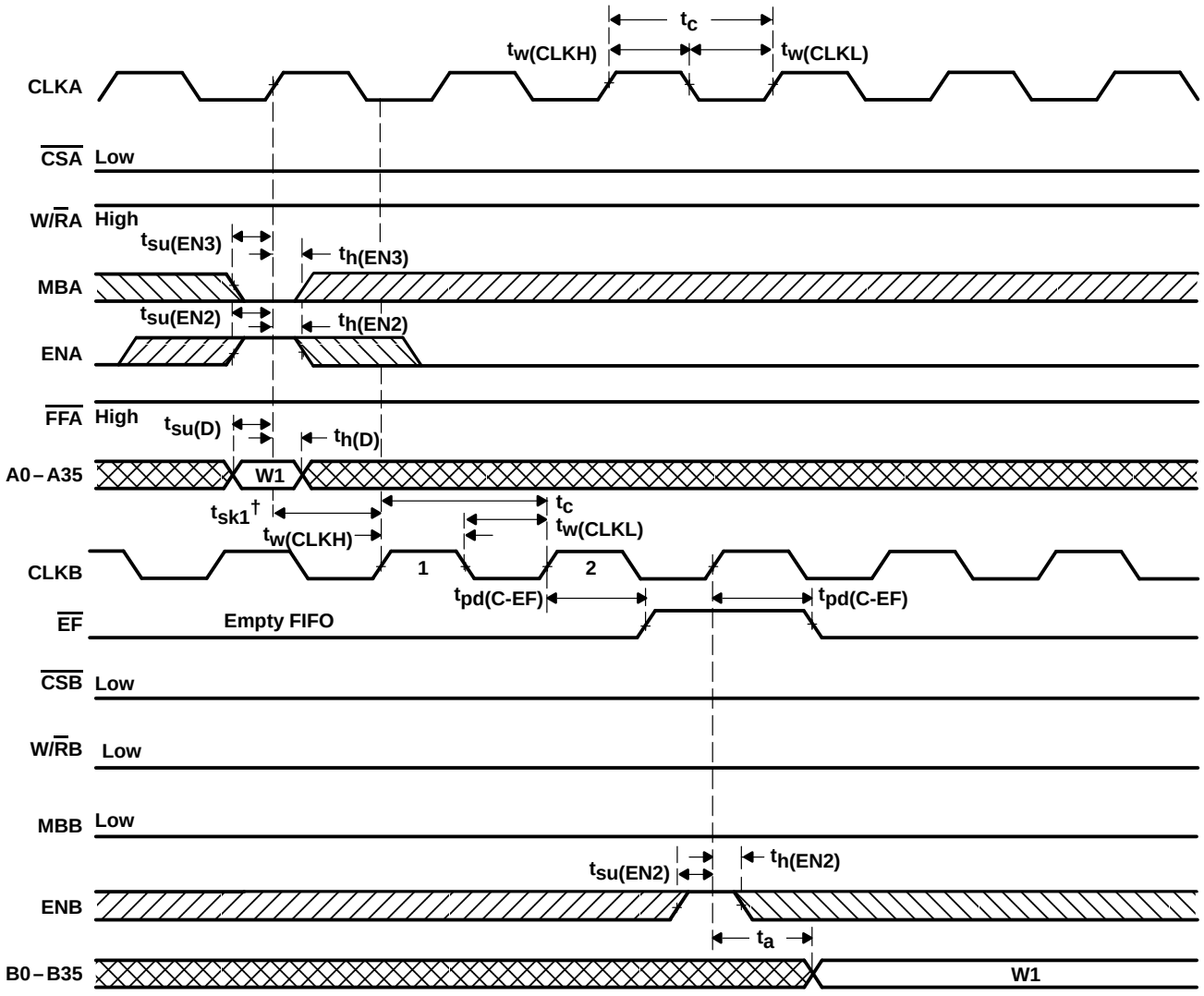
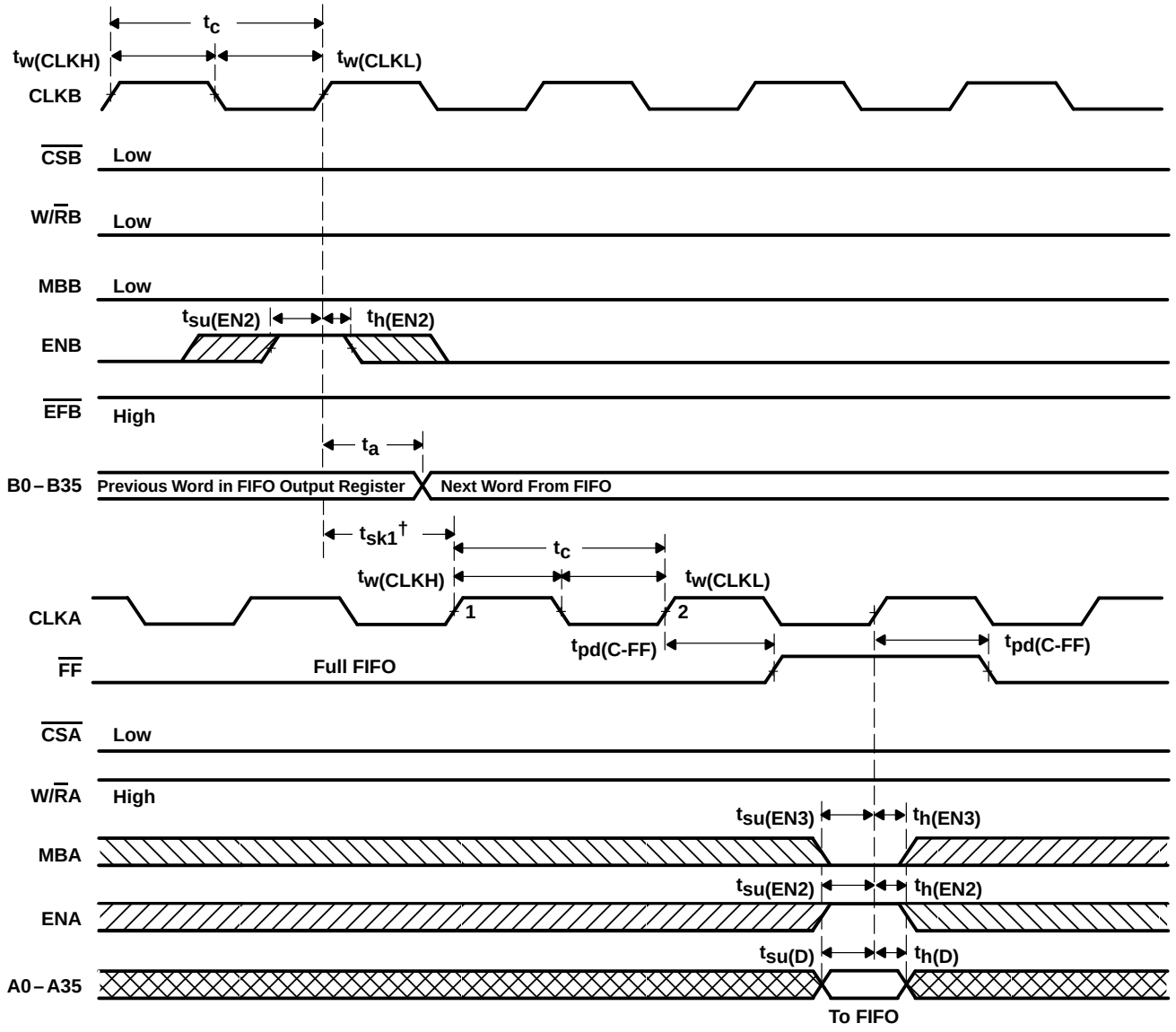


Figure 3. FIFO-Read-Cycle Timing



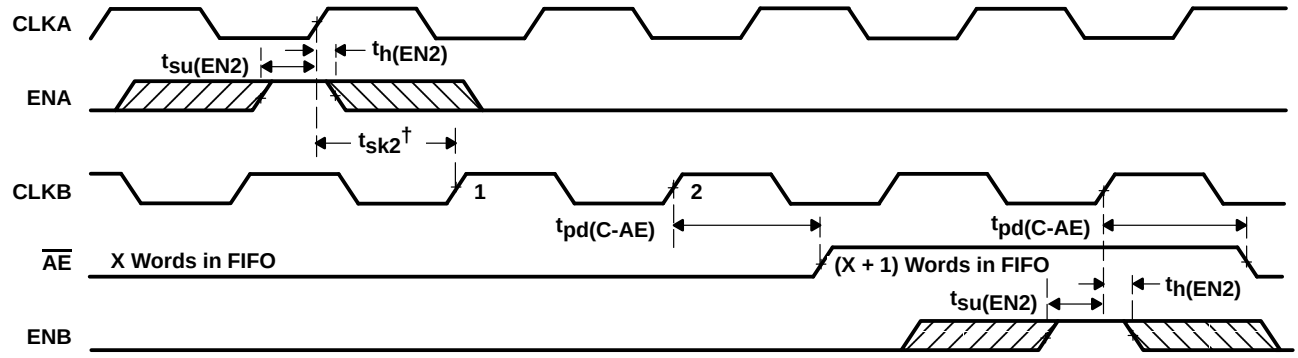
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of $\overline{EF}$ high may occur one CLKB cycle later than shown.

Figure 4. $\overline{EF}$-Flag Timing and First Data Read When the FIFO Is Empty



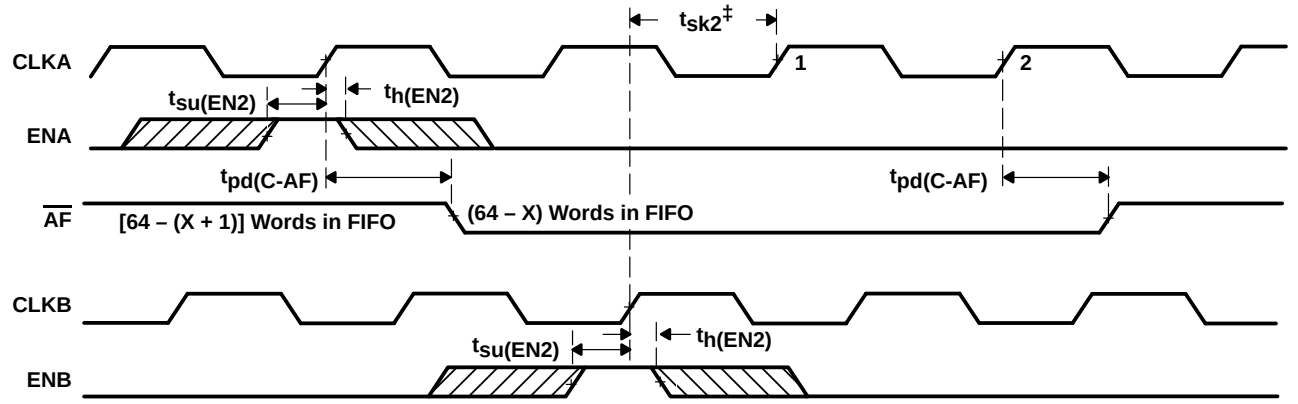
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less t_{sk1}, $\overline{FF}$ may transition high one CLKA cycle later than shown.

Figure 5. $\overline{FF}$-Flag Timing and First Available Write When the FIFO Is Full



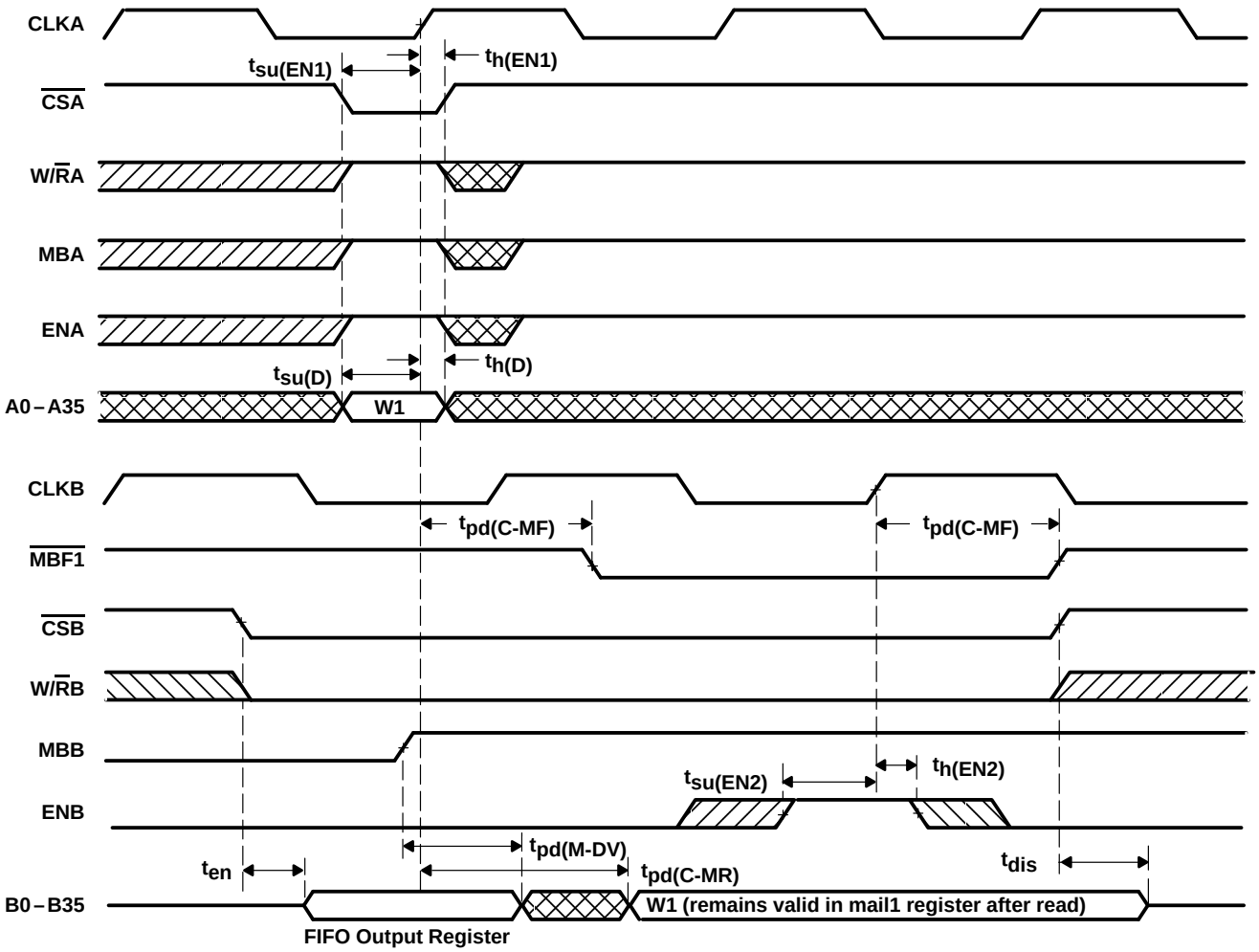
† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AE}$ may transition high one CLKB cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 6. Timing for $\overline{AE}$ When the FIFO Is Almost Empty



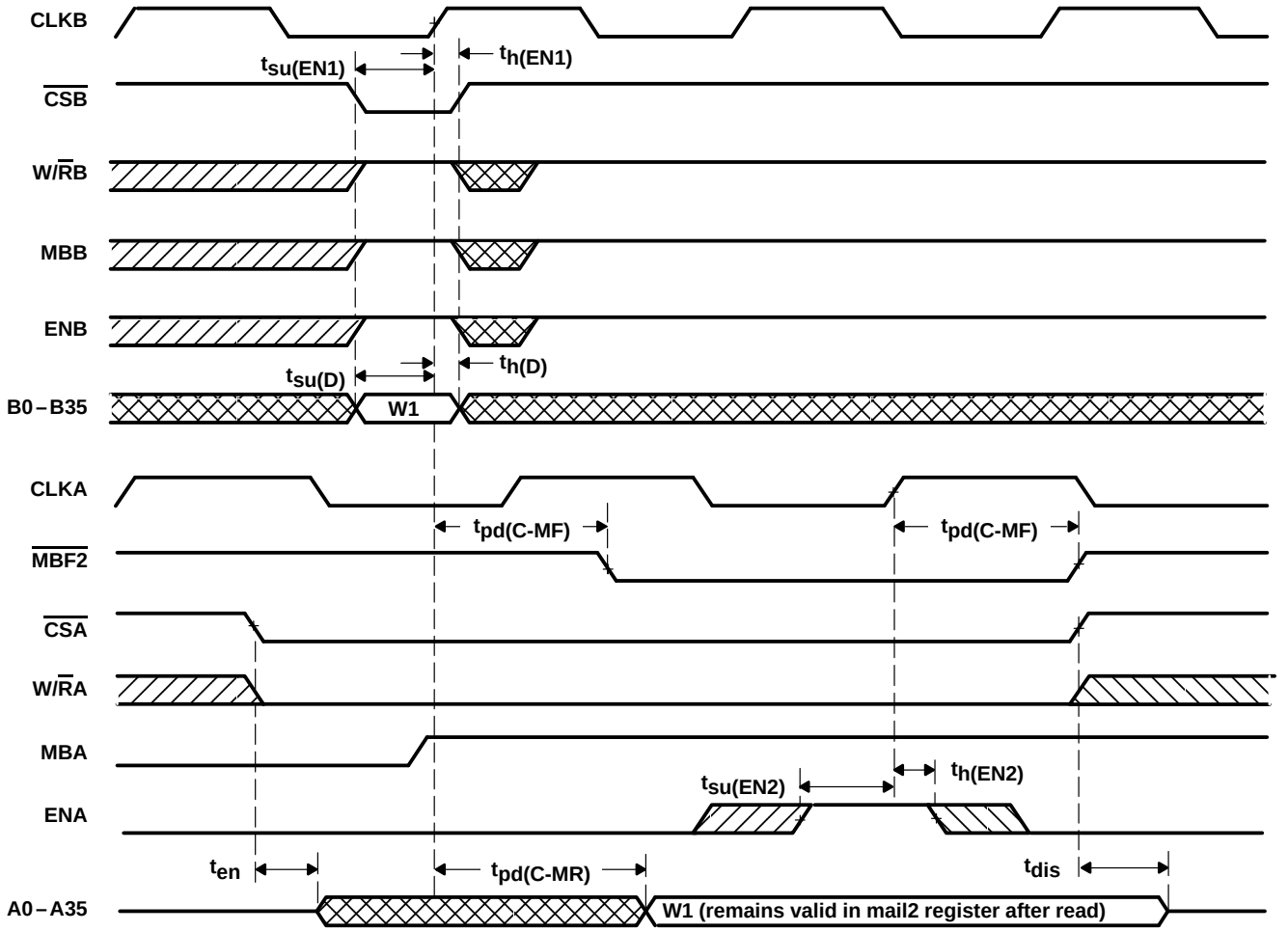
‡ t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AF}$ may transition high one CLKB cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 7. Timing for $\overline{AF}$ When the FIFO Is Almost Full



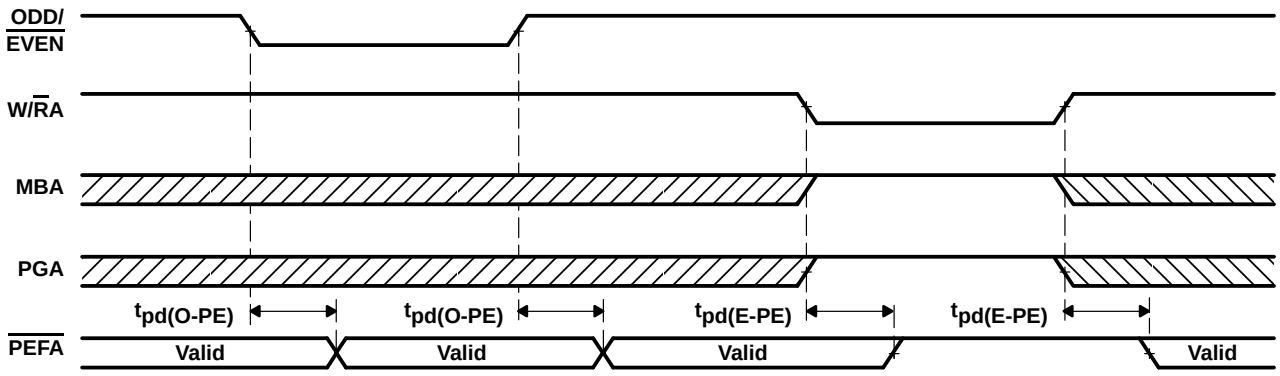
NOTE A: Port-B parity generation off (PGB = L)

Figure 8. Timing for Mail1 Register and $\overline{MBF1}$ Flag



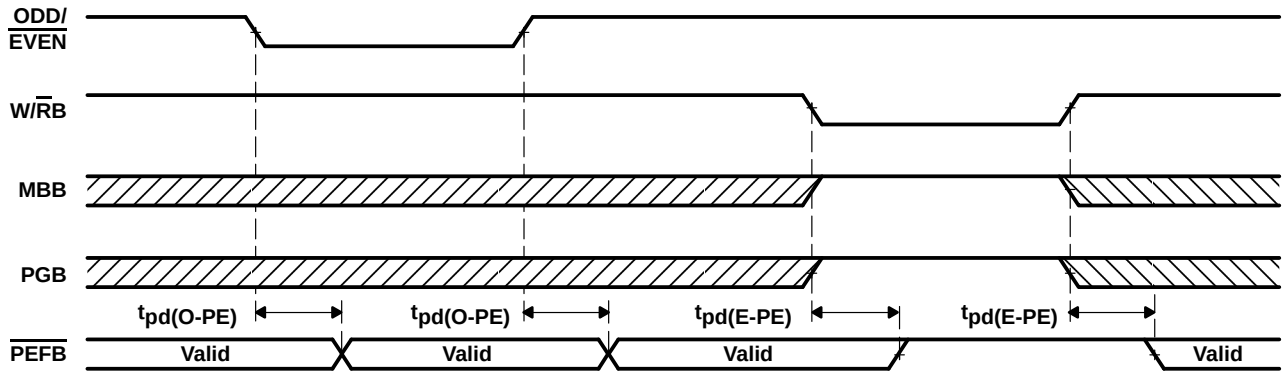
NOTE A: Port-A parity generation off (PGA = L)

Figure 9. Timing for Mail2 Register and $\overline{MBF2}$ Flag



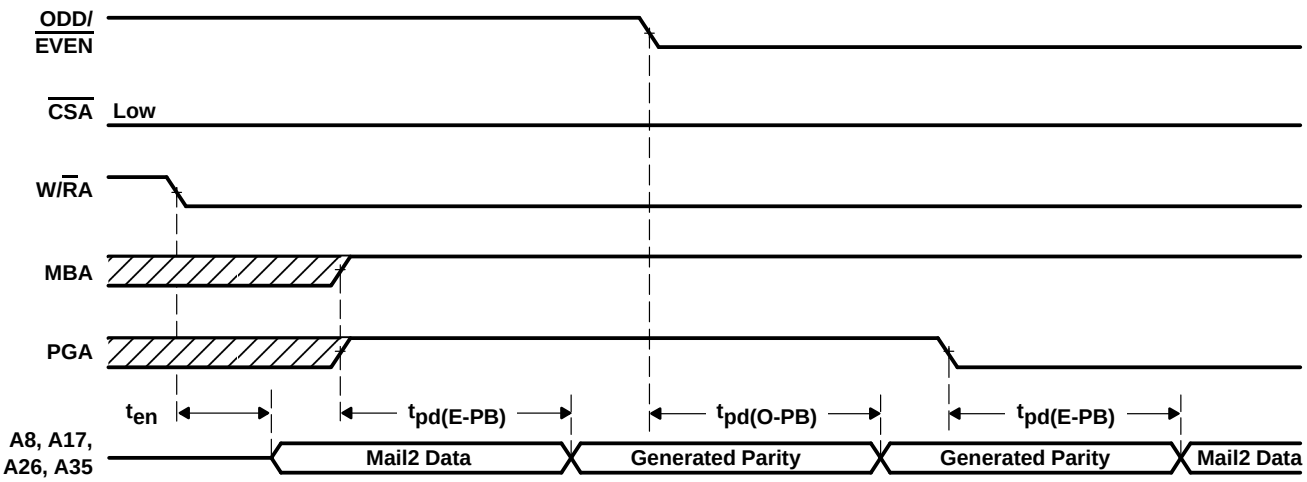
NOTE A: $\overline{CSA}$ = L and ENA = H

Figure 10. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



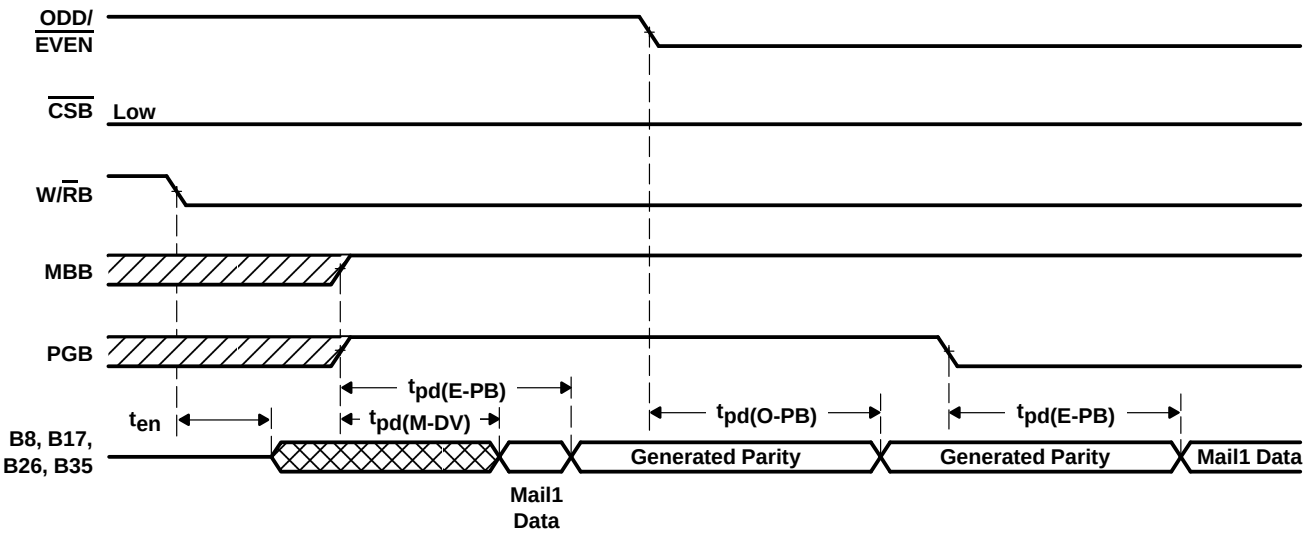
NOTE A: $\overline{CSB}$ = L and ENB = H

Figure 11. ODD/$\overline{EVEN}$, W/$\overline{RB}$, MBB, and PGB to $\overline{PEFB}$ Timing



NOTE A: ENA = H

Figure 12. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB = H

Figure 13. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±500 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±50	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	V_I = V_{CC} or GND	Outputs high			60	mA
				Outputs low			130	
				Outputs disabled			60	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 13)

		′ABT3611-15		′ABT3611-20		′ABT3611-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		MHz
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN1)}$	Setup time, $\overline{CSA}$, W/$\overline{R}$A before CLKA↑; $\overline{CSB}$, W/$\overline{R}$B, before CLKB↑	6		6		7		ns
$t_{su(EN2)}$	Setup time, ENA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(EN3)}$	Setup time, MBA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{EVEN}$ and PGB before CLKB↑†	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN1)}$	Hold time, $\overline{CSA}$, W/$\overline{R}$A after CLKA↑; $\overline{CSB}$, W/$\overline{R}$B after CLKB↑	1		1		1		ns
$t_{h(EN2)}$	Hold time, ENA after CLKA↑; ENB after CLKB↑	1		1		1		ns
$t_{h(EN3)}$	Hold time, MBA after CLKA↑; MBB after CLKB↑	1		1		1		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{EVEN}$ and PGB after CLKB↑†	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑‡	6		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	4		4		4		ns
t_{sk1}§	Skew time between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8		8		10		ns
t_{sk2}§	Skew time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9		16		20		ns

† Only applies for a rising edge of CLKB that does a FIFO read
‡ Requirement to count the clock edge as one of at least four needed to reset a FIFO
§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 13)

PARAMETER		′ABT3611-15		′ABT3611-20		′ABT3611-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C\text{-}FF)}$	Propagation delay time, CLKA↑ to $\overline{FF}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}EF)}$	Propagation delay time, CLKB↑ to $\overline{EF}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKB↑ to $\overline{AE}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{AF}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	12	3	14	3	16	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBB to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D\text{-}PE)}$	Propagation delay time, A0–A35 valid to $\overline{PEFA}$ valid; B0–B35 valid to $\overline{PEFB}$ valid	3	12	3	13	3	14	ns
$t_{pd(O\text{-}PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O\text{-}PB)}$§	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	2	15	ns
$t_{pd(E\text{-}PE)}$	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to $\overline{PEFB}$	1	12	1	13	1	15	ns
$t_{pd(E\text{-}PB)}$§	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to parity bits (B8, B17, B26, B35)	3	14	3	15	3	16	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{RST}$ to $\overline{AE}$ low and ($\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$) high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance	1	9	1	10	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
§ Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

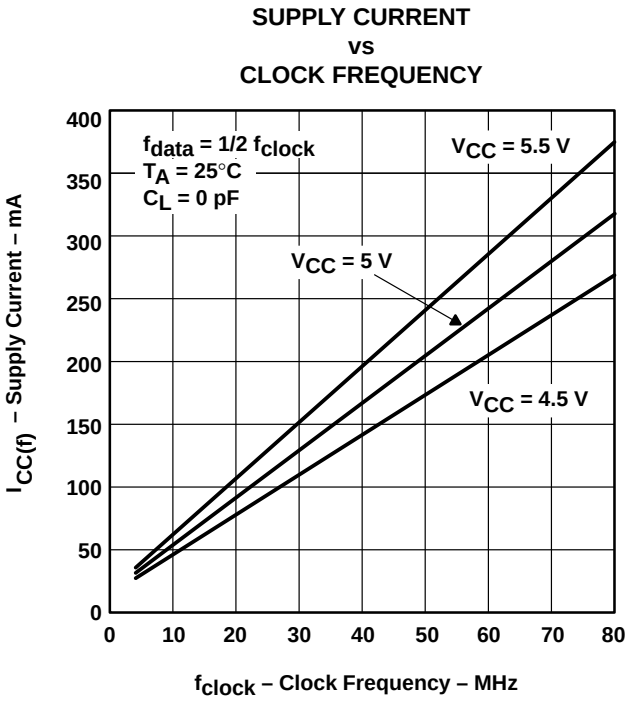


Figure 14

calculating power dissipation

The $I_{CC(f)}$ data for the graph was taken while simultaneously reading and writing the FIFO on the SN74ACT3611 with CLKA and CLKB operating at frequency f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 14, the maximum power dissipation (P_T) of the SN74ABT3611 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times (V_{OH} - V_{OL})^2 \times f_o)$$

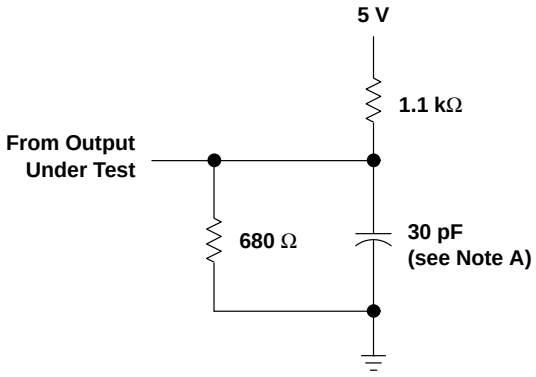
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = high-level output voltage
V_{OL} = low-level output voltage

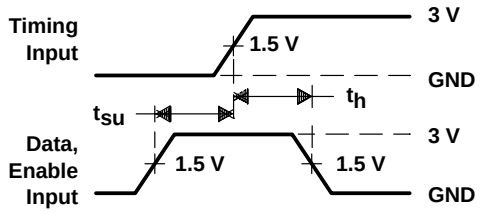
When no reads or writes are occurring on the SN74ABT3611, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.29 \text{ mA/MHz}$$

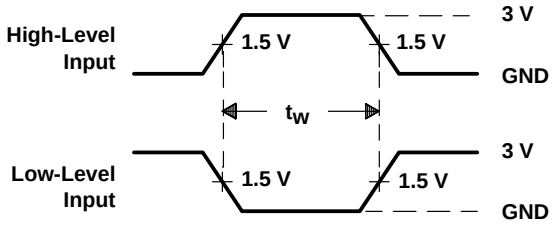
PARAMETER MEASUREMENT INFORMATION



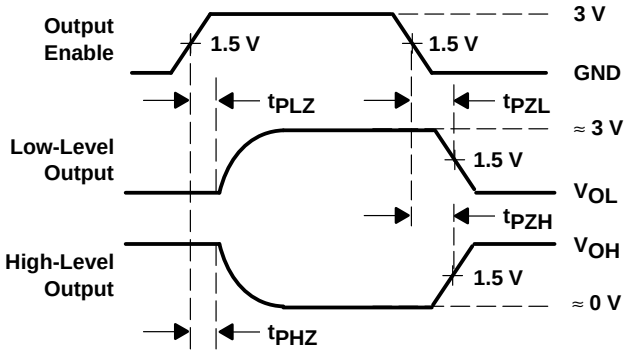
LOAD CIRCUIT



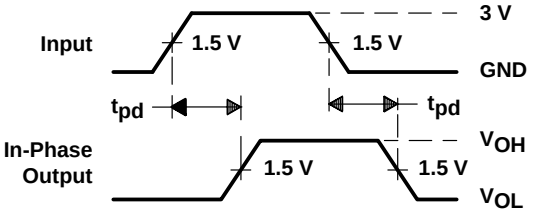
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 15. Load Circuit and Voltage Waveforms

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