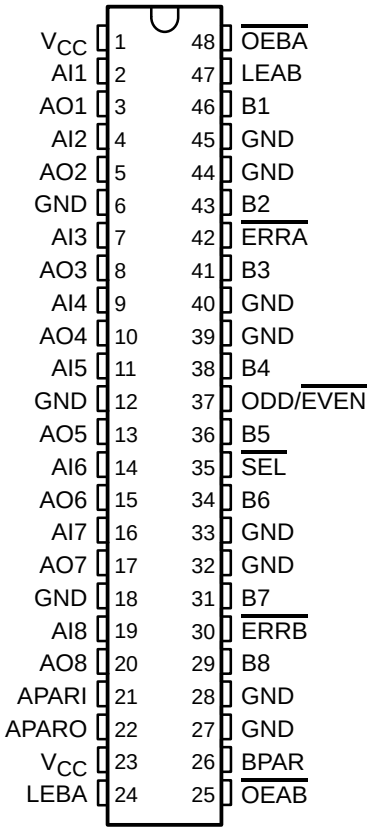
- **BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Support IEEE BTL Standard 1194.1-1991**
- **Open-Collector B Port Drives Load Impedances as Low as 10 Ω**
- **BTL Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Latchable Transceiver With Output Sink of 24 mA at the A Bus and 100 mA at the B Bus**
- **Option to Generate and Check Parity or Feed-Through Data/Parity in Directions A to B or B to A**
- **Independent Latch Enables for A-to-B and B-to-A Directions**
- **Select Pin for ODD/$\overline{\text{EVEN}}$ Parity**
- **$\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ Output Pins for Parity Checking**
- **Ability to Simultaneously Generate and Check Parity**
- **Packaged in 300-mil Plastic Shrink Small-Outline (DL) Package**

DL PACKAGE
(TOP VIEW)



description

The SN74BCT979 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver, or it can generate/check parity from the 8-bit data bus in either direction. It has a guaranteed current-sinking capability of 24 mA at the A bus and 100 mA at the open-collector B bus.

The SN74BCT979 features independent latch-enable (LEAB, LEBA) inputs for the A-to-B direction and the B-to-A direction, an ODD/$\overline{\text{EVEN}}$ input to select odd or even parity, and separate error-signal ($\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$) outputs for checking parity.

When communication between buses occurs, parity is generated and passed on to either bus as APARO or BPAR. Error detection of the parity generated from AI1–AI8 and B1–B8 can be checked by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$, providing LEAB and LEBA are high and the mode select ($\overline{\text{SEL}}$) is low. If $\overline{\text{SEL}}$ is high, the communication between buses is in a feed-through mode where parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$.

The SN74BCT979 features open-collector driver outputs (B port) with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω.

The transceiver has a precision threshold set by an internal bandgap reference to give accurate input thresholds over V_{CC} and temperature variations.

This transceiver is compatible with backplane transceiver logic (BTL) technology at significantly reduced power dissipation per channel.

The SN74BCT979 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OPERATION OR FUNCTION†
$\overline{OEAB}$	$\overline{OEBA}$	$\overline{SEL}$	LEAB	LEBA	
H	H	X	X	X	Isolation. AO1–AO8/APARO are in the high-impedance state and B1–B8/APAR are high.
H	L	L	X	H	Parity is generated from B1–B8 data and output on APARO and is checked against BPAR and output on $\overline{ERRB}$.
H	L	L	X	L	Parity is generated from latched B1–B8 data and output on APARO and is checked against BPAR and output on $\overline{ERRB}$.
H	L	H	X	H	BPAR is output on APARO. Parity is generated from B1–B8 data, checked against BPAR, and output on $\overline{ERRB}$.
H	L	H	X	L	BPAR is output on APARO. Parity is generated from latched B1–B8 data, checked against BPAR, and output on $\overline{ERRB}$.
L	H	L	H	X	Parity is generated from AI1–AI8 data and output on BPAR and is checked against APARI and output on $\overline{ERRA}$.
L	H	L	L	X	Parity is generated from latched AI1–AI8 data and output on BPAR and is checked against APARI and output on $\overline{ERRA}$.
L	H	H	H	X	APARI is output on BPAR. Parity is generated from AI1–AI8 data, checked against APARI, and output on $\overline{ERRA}$.
L	H	H	L	X	APARI is output on BPAR. Parity is generated from latched AI1–AI8 data, checked against APARI, and output on $\overline{ERRA}$.
L	L	X	X	X	AO1–AO8/APARO and B1–B8/BPAR are active (high or low logic levels).

† Parity is generated from AI1–AI8 and from B1– B8 based on the level present at ODD/$\overline{EVEN}$. Parity is checked (AI1– AI8 against APARI and B1–B8 against BPAR) based on the level present at ODD/$\overline{EVEN}$ (see parity function table).

PARITY FUNCTION TABLE‡

INPUTS					OUTPUTS	
$\overline{OEAB}$	$\overline{SEL}$	ODD/$\overline{EVEN}$	Σ OF INPUTS AI1–AI8 = H	APARI	BPAR	$\overline{ERRA}$
L	L	L	0, 2, 4, 6, 8	L	L	H
L	L	L	1, 3, 5, 7	L	H	L
L	L	L	0, 2, 4, 6, 8	H	L	L
L	L	L	1, 3, 5, 7	H	H	H
L	L	H	0, 2, 4, 6, 8	L	H	L
L	L	H	1, 3, 5, 7	L	L	H
L	L	H	0, 2, 4, 6, 8	H	H	H
L	L	H	1, 3, 5, 7	H	L	L
L	H	L	0, 2, 4, 6, 8	L	L	H
L	H	L	1, 3, 5, 7	L	L	L
L	H	L	0, 2, 4, 6, 8	H	H	L
L	H	L	1, 3, 5, 7	H	H	H
L	H	H	0, 2, 4, 6, 8	L	L	L
L	H	H	1, 3, 5, 7	L	L	H
L	H	H	0, 2, 4, 6, 8	H	H	H
L	H	H	1, 3, 5, 7	H	H	L
H	X	X	X	X	H	X

‡ Parity functions for the A bus are shown. Parity functions for the B bus are similar, but use B1–B8 and BPAR as inputs and APARO and $\overline{ERRB}$ as outputs.

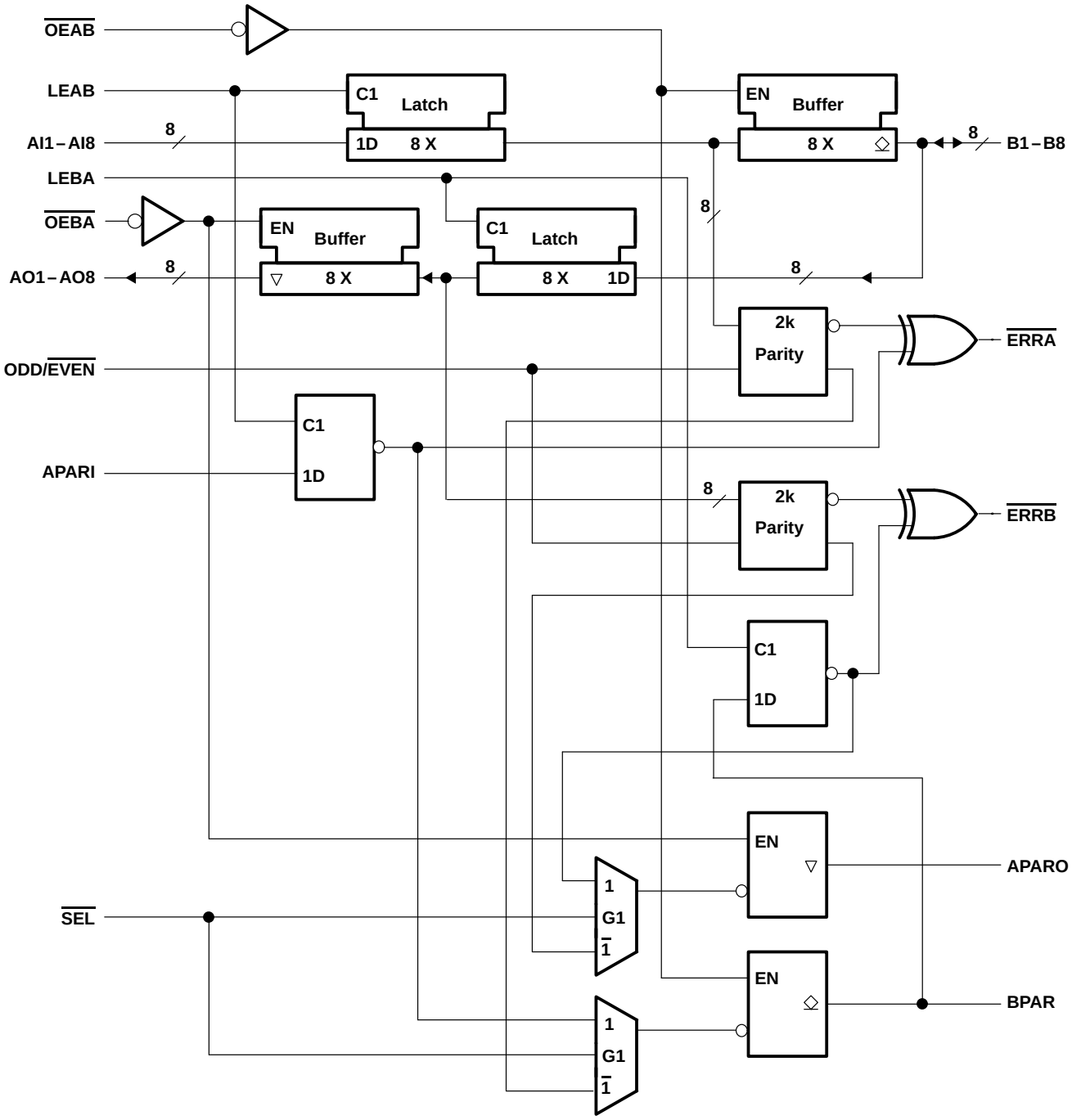
LATCH FUNCTION TABLES

INPUTS†			OUTPUT
$\overline{OEAB}$	LEAB	AI	B
L	H	L	L
L	H	H	H
L	L	X	Q_0
H	X	X	H

INPUTS†			OUTPUT
$\overline{OEBA}$	LEBA	B	AO
L	H	L	L
L	H	H	H
L	L	X	Q_0
H	X	X	Z

† If LEAB = H, current AI1 – AI8 and APARI data is used. If LEAB = L, latched AI1 – AI8 and APARI data is used.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1): B1–B8, BPAR . . . . . –0.5 V to 5.5 V
Other inputs . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) (A port) . . . . . –30 mA
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 200 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Maximum power dissipation at T_A = 55°C (in still air) . . . . . 0.85 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	B1–B8, BPAR	1.6			V
		Other inputs	2			
V_{IL}	Low-level input voltage	B1–B8, BPAR			1.47	V
		Other inputs			0.8	
V_{OH}	High-level output voltage	B1–B8, BPAR			2.1	mA
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO1–AO8, APARO, $\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$			–3	mA
I_{OL}	Low-level output current	AO1–AO8, APARO, $\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$			24	mA
		B1–B8, BPAR			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	LE, $\overline{OE}$, $\overline{SEL}$, ODD/$\overline{EVEN}$, AI1–AI8, APARI	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
I_{OH}	B1–B8, BPAR	V_{CC} = 5.5 V,	V_{OH} = 2.1 mA			100	µA
V_{OH}	AO1–AO8, APARO, $\overline{ERRA}$, $\overline{ERRB}$	V_{CC} = 4.5 V	I_{OH} = –1 mA	2.5	3.4		V
			I_{OH} = – 3 mA	2.4	3.3		
V_{OL}	AO1–AO8, APARO, $\overline{ERRA}$, $\overline{ERRB}$	V_{CC} = 4.5 V	I_{OL} = 24 mA		0.35	0.5	V
			I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA	0.75		1.15	
I_I	LE, $\overline{OE}$, $\overline{SEL}$, ODD/$\overline{EVEN}$, AI1–AI8, APARI	V_{CC} = 5.5 V,	V_I = 5.5 V			100	µA
I_{IH}	LE, $\overline{OE}$, $\overline{SEL}$, ODD/$\overline{EVEN}$, AI1–AI8, APARI	V_{CC} = 5.5 V	V_I = 2.7 V			20	µA
	B1–B8, BPAR‡		V_I = 2.1 V			100	
I_{IL}	LE, $\overline{OE}$, $\overline{SEL}$, ODD/$\overline{EVEN}$, AI1–AI8, APARI	V_{CC} = 5.5 V	V_I = 0.5 V			–20	µA
	B1–B8, BPAR‡		V_I = 0.3 V			–100	
I_{OZH}	AO1–AO8, APARO	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO1–AO8, APARO	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OS}§	AO1–AO8, APARO	V_{CC} = 5.5 V,	V_O = 0	–60		–200	mA
I_{CC}	Outputs high	V_{CC} = 5.5 V,	Outputs open		17	36	mA
	Outputs low				69	85	
	Outputs disabled				21	42	
C_i	LE, $\overline{OE}$, $\overline{SEL}$, ODD/$\overline{EVEN}$	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		8		pF
	AI1–AI8, APARI				8		
C_{io}	B1–B8, BPAR	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		5		pF
C_o	AO1–AO8, APARO	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		6.5		pF
T_T	Output transition time	B port¶			1		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ Measured from 1.3 V to 1.8 V (see Figure 1).

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t_w	Pulse duration		LEAB high	5		5		ns
			LEBA high	4		4		
t_{su}	Setup time	AI1–AI8, APARI before LEAB↓	Data high	4		4		ns
			Data low	3		3		
		B1–B8, BPAR before LEBA↓	Data high	8.5		8.5		
			Data low	7		7		
t_h	Hold time	AI1–AI8, APARI after LEAB↓	Data high	1		1		ns
			Data low	2.5		2.5		
		B1–B8, BPAR after LEBA↓	Data high	0.5		0.5		
			Data low	0.5		0.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	AI	B	1.3	6.8	8.6	1.3	10.4	ns
t_{PHL}			2.1	7.8	9.8	2.1	11.8	
t_{PLH}	AI	BPAR	3.7	11.6	13.9	3.7	17.6	ns
t_{PHL}			5.4	13.9	15.7	5.4	19.2	
t_{PLH}	B	AO	2.8	9	11.1	2.8	14.3	ns
t_{PHL}			2.4	8.1	10	2.4	12.3	
t_{PLH}	B	APARO	4.5	14.1	16.1	4.5	20.9	ns
t_{PHL}			4.2	13.3	15.9	4.2	20.5	
t_{PLH}	APARI	BPAR	1.6	6	7.7	1.6	9.3	ns
t_{PHL}			3.4	9.5	11.2	3.4	13.6	
t_{PLH}	BPAR	APARO	2.7	7.9	9.9	2.7	12.8	ns
t_{PHL}			3	8.1	10	3	12.5	
t_{PLH}	AI	$\overline{ERRA}$	3	10.9	13	3	16.1	ns
t_{PLH}	APARI		2.8	8.2	10.2	2.8	12.6	
t_{PHL}	AI	$\overline{ERRA}$	4.2	11.8	14	4.2	16.7	ns
t_{PHL}	APARI		4	8.9	10.9	4	12.8	
t_{PLH}	B	$\overline{ERRB}$	4.3	13.4	15.9	4.3	20.6	ns
t_{PLH}	BPAR		4.2	10.8	13.1	4.2	16.6	
t_{PHL}	B	$\overline{ERRB}$	5.5	14.5	17	5.5	21.5	ns
t_{PHL}	BPAR		5.5	11.3	13.5	5.5	16.5	
t_{PLH}	ODD/$\overline{EVEN}$	$\overline{ERRA}$	3.4	9.1	10.9	3.4	13.7	ns
t_{PHL}			4.4	10.3	12.2	4.4	14.5	
t_{PLH}	ODD/$\overline{EVEN}$	$\overline{ERRB}$	3.4	8.7	10.7	3.4	13.3	ns
t_{PHL}			4.6	10	11.9	4.6	14.2	
t_{PLH}	ODD/$\overline{EVEN}$	APARO	3.4	8.7	10.6	3.4	13.5	ns
t_{PHL}			3.1	9	10.9	3.1	13.4	
t_{PLH}	ODD/$\overline{EVEN}$	BPAR	4	10.3	12.1	4	15.8	ns
t_{PHL}			4.9	12.3	14.1	4.9	17.3	
t_{PLH}	$\overline{SEL}$	APARO	0.7	5.3	6.9	0.7	8.4	ns
t_{PHL}			1.1	5	6.5	1.1	7.8	
t_{PLH}	$\overline{SEL}$	BPAR	1.1	6.4	8.1	1.1	10.1	ns
t_{PHL}			2.8	8.3	9.9	2.8	12.6	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 3) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	LEAB	B	1.6	7.6	9.5	1.6	11.6	ns
t_{PHL}			2.7	8.1	10	2.7	11.7	
t_{PLH}	LEAB	BPAR (parity feed through)	2.3	7.3	9.2	2.3	10.8	ns
t_{PHL}			4.6	9.3	11	4.6	13.3	
t_{PLH}	LEAB	BPAR (parity generated)	4.7	10.7	13	4.7	16.2	ns
t_{PHL}			6.2	11.5	13.4	6.2	16	
t_{PLH}	LEAB	$\overline{ERRA}$	3.3	8.6	10.7	3.3	12.8	ns
t_{PHL}			4.7	9.8	12	4.7	13.7	
t_{PLH}	LEBA	AO	1.3	6.5	8.5	1.3	10	ns
t_{PHL}			1.4	5.9	7.6	1.4	8.5	
t_{PLH}	LEBA	APARO (parity feed through)	1.7	5.9	7.7	1.7	9.1	ns
t_{PHL}			1.9	6	7.8	1.9	9	
t_{PLH}	LEBA	APARO (parity generated)	3.5	9.3	11.5	3.5	14.1	ns
t_{PHL}			3.1	8.2	10.3	3.1	12.2	
t_{PLH}	LEBA	$\overline{ERRB}$	3.4	8.7	10.8	3.4	12.7	ns
t_{PHL}			4.6	9	11	4.6	12.5	
t_{PLH}	$\overline{OEAB}$	B	1.5	5.5	7	1.5	7.9	ns
t_{PHL}			4.9	10.4	12.1	4.9	14.1	
t_{PLH}	$\overline{OEAB}$	BPAR	1.4	5.4	6.9	1.4	7.8	ns
t_{PHL}			4.8	10.6	12.5	4.8	14.9	
t_{PZH}	$\overline{OEBA}$	AO	1.4	6	7.8	1.4	9.2	ns
t_{PZL}			6	10.7	12.5	6	14.6	
t_{PHZ}	$\overline{OEBA}$	AO	2.4	6.7	8.6	2.4	9.5	ns
t_{PLZ}			1.2	4.7	6.3	1.2	7.1	
t_{PZH}	$\overline{OEBA}$	APARO	1.7	6.1	7.8	1.7	9.3	ns
t_{PZL}			1.4	5.1	6.7	1.4	7.8	
t_{PHZ}	$\overline{OEBA}$	APARO	2.7	6.8	8.6	2.7	9.5	ns
t_{PLZ}			1.2	4.7	6.2	1.2	7.1	

NOTE 3: Load circuits and waveforms are shown in Section 1.

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