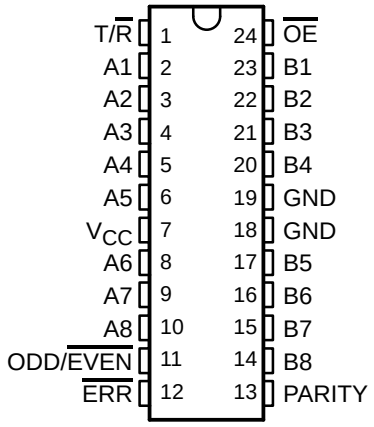
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **High-Impedance State During Power Up and Power Down**
- **3-State B Outputs Sink 64 mA and Source 15 mA**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN64BCT657 contains eight noninverting buffers with parity generator/checker circuits and control signals. The transmit/receive (T/$\overline{R}$) input determines the direction of data flow. When T/$\overline{R}$ is high, data flows from the A port to the B port (transmit mode); when T/$\overline{R}$ is low, data flows from the B port to the A port (receive mode). When the output-enable ($\overline{OE}$) input is high, both the A and B ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level on the ODD/$\overline{EVEN}$ input. PARITY carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the A bus is polled to determine the number of high bits, PARITY is set to the logic level that maintains the parity sense selected by the level at the ODD/$\overline{EVEN}$ input. For example, if ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the A bus, then PARITY is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

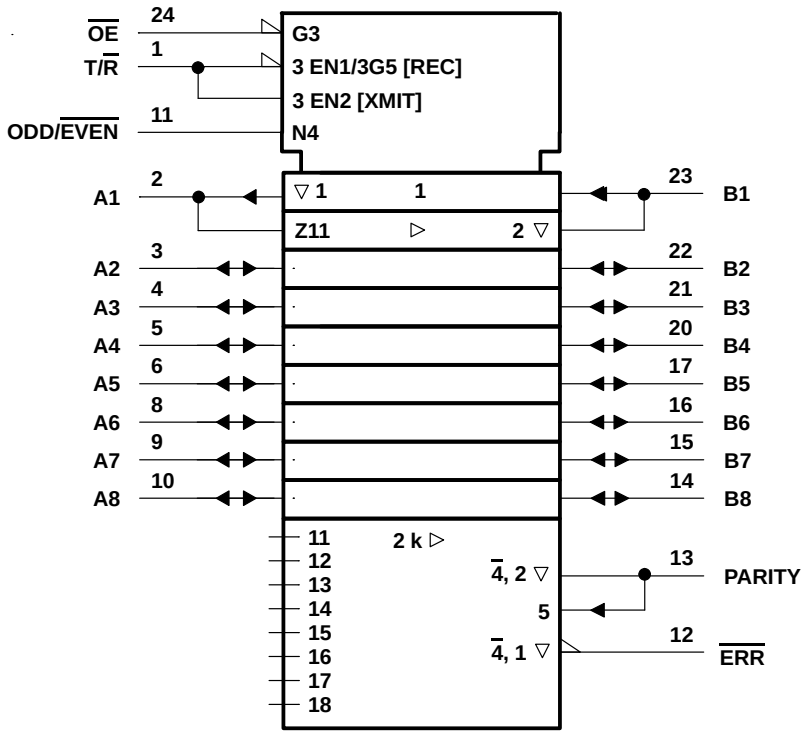
In the receive mode, after the B bus is polled to determine the number of high bits, the error ($\overline{ERR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if ODD/$\overline{EVEN}$ is high (odd parity selected), PARITY is high, and there are three high bits on the B bus, then $\overline{ERR}$ is low, indicating a parity error.

The SN64BCT657 is characterized for operation from –40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE

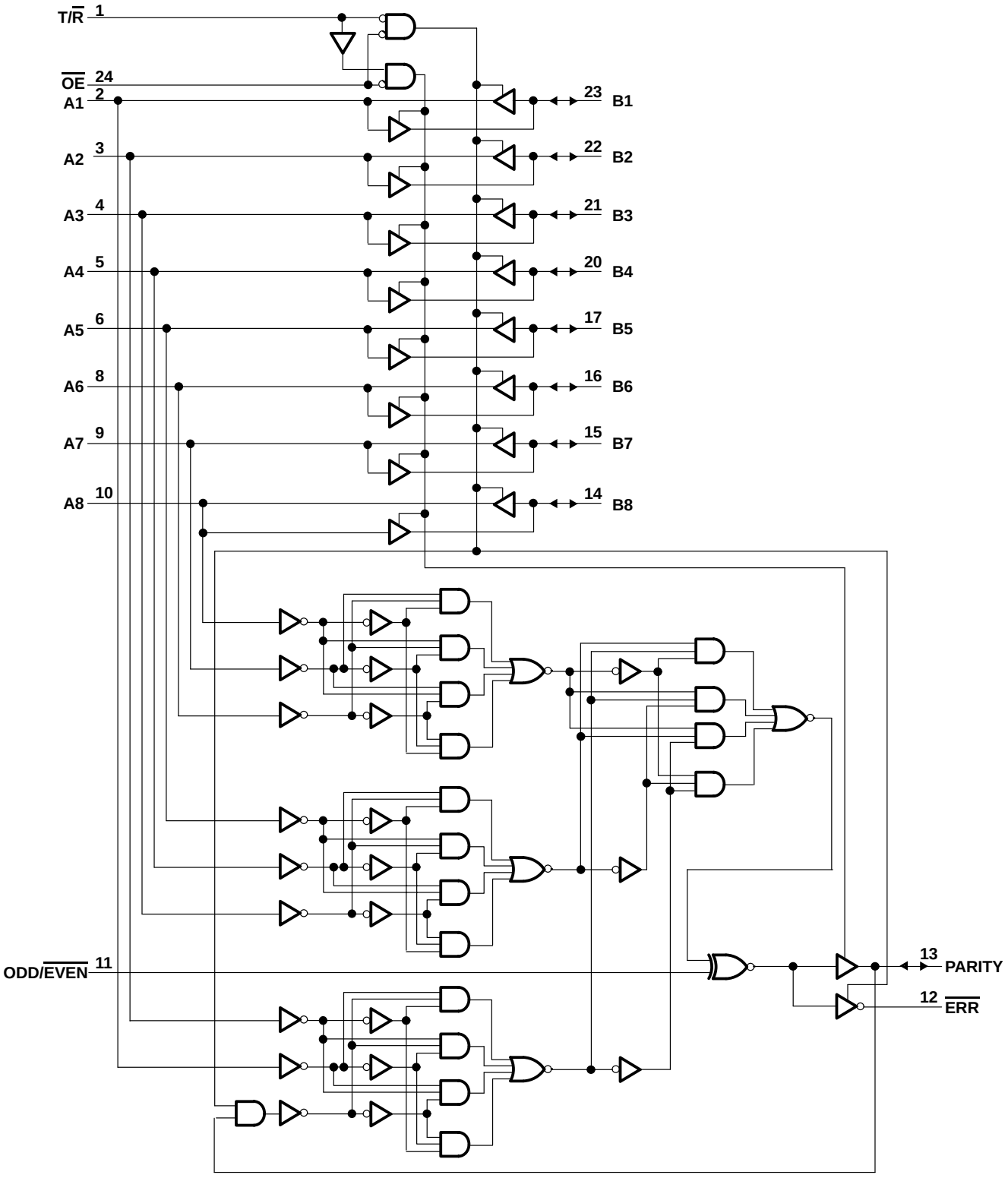
NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . –30 mA
Current into any output in the low state, I_O . . . . . 60 mA
Operating free-air temperature range . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–3	mA
		B port, PARITY, $\overline{ERR}$			–15	
I_{OL}	Low-level output current	A port			24	mA
		B port, PARITY, $\overline{ERR}$			64	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		2			μs/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	Any output	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.4	3.3		V
	B port, PARITY, $\overline{ERR}$	V_{CC} = 4.5 V,	I_{OH} = –15 mA		2	3.1		
	Any output	V_{CC} = 4.75 V,	I_{OH} = – 3 mA		2.7			
V_{OL}	A port	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.35	0.5	V
	B port, PARITY, $\overline{ERR}$	V_{CC} = 4.5 V,	I_{OL} = 64 mA			0.42	0.55	
I_I	T/$\overline{R}$	V_{CC} = 0,	V_I = 7 V	$\overline{OE}$ = 4.5 V			20	µA
	$\overline{OE}$			T/$\overline{R}$ = 4.5 V			20	
	ODD/$\overline{EVEN}$	V_{CC} = 0,	V_I = 7 V				20	
	A port	V_{CC} = 0 to 5.5 V,	V_I = 5.5 V				100	
	B port, PARITY						200	
I_{IH}‡	A or B port, PARITY	V_{CC} = 5.5 V,	V_I = 2.7 V				200	µA
	T/$\overline{R}$, $\overline{OE}$						20	
	ODD/$\overline{EVEN}$						20	
I_{IL}‡	A or B port, PARITY	V_{CC} = 5.5 V,	V_I = 0.5 V				–70	µA
	T/$\overline{R}$, $\overline{OE}$						–20	
	ODD/$\overline{EVEN}$						–20	
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0		–60		–200	mA
	B port, PARITY, $\overline{ERR}$				–125		–300	
I_{OZH}	$\overline{ERR}$	V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}	$\overline{ERR}$	V_{CC} = 5.5 V,	V_O = 0.5 V				–50	µA
I_{CCL}		V_{CC} = 5.5 V,	Outputs open				90	mA
I_{CCH}		V_{CC} = 5.5 V,	Outputs open				2	mA
I_{CCZ}		V_{CC} = 5.5 V,	Outputs open				1	mA
C_i	Control inputs	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			6.5		pF
C_{io}	A port	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V			10		pF
	B port, PARITY					14		
C_o	$\overline{ERR}$	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics over recommended range of supply voltage, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			T_A = –40°C to 85°C		T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.1	3.1	6	1.1	6.9	1.1	6.6	ns
t_{PHL}			2	5.3	8.5	2	9.3	2	9	
t_{PLH}	A	PARITY	3	7.4	12.7	3	16.4	3	15.4	ns
t_{PHL}			4.6	8.6	14.1	4.6	16.9	4.6	15.9	
t_{PLH}	ODD/$\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	1.1	4.1	6.4	1.1	7.7	1.1	7.1	ns
t_{PHL}			2.6	5.5	8.3	2.6	9.3	2.6	9	
t_{PLH}	B	$\overline{\text{ERR}}$	3.1	7.4	12.6	3.1	16.4	3.1	15.3	ns
t_{PHL}			4.4	6.5	13.3	4.4	16.6	4.4	15.5	
t_{PLH}	PARITY	$\overline{\text{ERR}}$	3.4	7.7	10.7	3.4	14.4	3.4	13.2	ns
t_{PHL}			5.5	8.8	12	5.5	14.9	5.5	13.9	
t_{PZH}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	1.8	5.1	7.7	1.8	9.5	1.8	9.1	ns
t_{PZL}			3.2	6.7	14.2	3.2	17	3.2	16.3	
t_{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	2.6	5.7	8	2.6	9.5	2.6	9.1	ns
t_{PLZ}			2	5	7.4	2	8.8	2	8	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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