### SN74BCT657 OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER

AND 3-STATE OUTPUTS SCBS079B – NOVEMBER 1991 – REVISED APRIL 1994

	SCBS079B – NOVEMBER 1991 – RE	.VIS
<ul> <li>State-of-the-Art BiCMOS Design Significantly Reduces I<sub>CCZ</sub></li> </ul>	DW OR NT PACKAGE (TOP VIEW)	
<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)</li> </ul>	T/R [ 1 24] OE A1 [ 2 23] B1 A2 [ 3 22] B2 A3 [ 4 21] B3	
<ul> <li>3-State B Outputs Sink 48 mA or 64 mA and Source 12 mA or 15 mA</li> </ul>	A4 [ 5 20 ] B4 A5 [ 6 19 ] GND	
<ul> <li>Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)</li> </ul>	V <sub>CC</sub> [ 7 18 ] GND A6 [ 8 17 ] B5 A7 [ 9 16 ] B6	
description	A8 [ 10 15 ] B7 ODD/EVEN [ 11 14 ] B8	
The SN74BCT657 contains eight noninverting	ERR [] 12 13 ]] PARITY	

The SN74BCT657 contains eight noninverting transceivers with 3-state outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications.

The transmit/receive  $(T/\overline{R})$  input determines the direction of the data flow through the bidirectional transceivers. When  $T/\overline{R}$  is high, data is transmitted from the A port to the B port. When  $T/\overline{R}$  is low, data is received at the A port from the B port.

When the output-enable  $(\overline{OE})$  input is high, both the A and B ports are placed in a high-impedance state (disabled). The ODD/EVEN input allows the user to select between odd or even parity systems.

When transmitting from A port to B port (T/ $\overline{R}$  high), PARITY is an output from the generator/checker. When receiving from B port to A port (T/ $\overline{R}$  low), PARITY is an input.

When transmitting (T/R high), the parity-select (ODD/ $\overline{EVEN}$ ) input is made high or low as appropriate. The A port is then polled to determine the number of high bits. The PARITY output goes to the logic state determined by the parity-select (ODD/ $\overline{EVEN}$ ) input and the number of high bits on A port. When ODD/ $\overline{EVEN}$  is low (for even parity) and the number of high bits on A port is odd, the PARITY will be high, transmitting even parity. If the number of high bits on A port is even, the PARITY will be low, keeping even parity.

When in the receive mode (T/R low), the B port is polled to determine the number of high bits. If ODD/EVEN is low (for even parity) and the number of highs on B port is as follows:

- Odd and the PARITY input is high, then ERR will be high signifying no error.
- Even and the PARITY input is high, then ERR will be low indicating an error.

The SN74BCT657 is characterized for operation from 0°C to 70°C.



### SN74BCT657 OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SCBS079B - NOVEMBER 1991 - REVISED APRIL 1994

FUNCTION TABLE								
NUMBER OF A OR B	INPUTS			INPUT/OUTPUT	OUTPUTS			
INPUTS THAT ARE HIGH	OE	T/R	ODD/EVEN	PARITY	ERR	OUTPUT MODE		
	L	Н	н	н	Z	Transmit		
	L	Н	L	L	Z	Transmit		
0.2.4.6.9	L	L	н	н	н	Receive		
0, 2, 4, 6, 8	L	L	н	L	L	Receive		
	L	L	L	н	L	Receive		
	L	L	L	L	Н	Receive		
	L	Н	н	L	Z	Transmit		
	L	Н	L	н	Z	Transmit		
4 9 5 7	L	L	н	н	L	Receive		
1, 3, 5, 7	L	L	н	L	н	Receive		
	L	L	L	н	н	Receive		
	L	L	L	L	L	Receive		
Don't care	Н	Х	Х	Z	Z	Z		

logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



# logic diagram (positive logic)





## SN74BCT657 OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SCBS079B - NOVEMBER 1991 - REVISED APRIL 1994

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the disabled or power-off state, $V_{O}$	
Voltage range applied to any output in the high state, $V_{O}$	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Current into any output in the low state, I <sub>O</sub>	
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

				NOM	MAX	UNIT	
VCC	Supply voltage			5	5.5	V	
VIH	High-level input voltage					V	
VIL	Low-level input voltage				0.8	V	
IIK	Input clamp current				-18	mA	
ЮН	High-level output current	A port			-3	mA	
		B port, PARITY, ERR			-15	ША	
IOL		A port			24	mA	
	Low-level output current B port, PARITY, ERR				64	ША	
TA	Operating free-air temperature				70	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



# **SN74BCT657** OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER

AND 3-STATE OUTPUTS SCBS079B – NOVEMBER 1991 – REVISED APRIL 1994

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK		V <sub>CC</sub> = 4.5 V,	lj = -18 mA				-1.2	V
	Any output	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.4	3.3		
Vон	B port, PARITY, ERR	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -15 mA		2	3.1		V
	Any output	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -3 mA		2.7			
	A port	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA			0.35	0.5	V
VOL	B port, PARITY, ERR	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA			0.42	0.55	v
	T/R	V <sub>CC</sub> = 0,	V <sub>I</sub> = 7 V,	OE = 4.5 V			20	
	OE	V <sub>CC</sub> = 0,	V <sub>I</sub> = 7 V,	T/ <del>R</del> = 4.5 V			20	
lj –	ODD/EVEN	V <sub>CC</sub> = 0,	V <sub>I</sub> = 7 V				20	μA
	A port						100	
	B port, PARITY	V <sub>CC</sub> = 5.5 V,	VI =55.9 v				200	
	A or B port, PARITY	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V				200	
IIH‡	T/R, OE						20	μA
	ODD/EVEN					20		
	A or B port, PARITY	V <sub>CC</sub> = 5.5 V,	Vj = 0.5 V				-70	
IIL‡	T/R, OE						-20	μA
	ODD/EVEN						-20	
6	A port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0		-60		-200	
los§	B port, PARITY, ERR				-125		-300	mA
IOZH	ERR	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	μA
IOZL	ERR	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	μA
ICCL	•	V <sub>CC</sub> = 5.5 V,	Outputs open				90	mA
ІССН		V <sub>CC</sub> = 5.5 V,	Outputs open				2	mA
ICCZ		V <sub>CC</sub> = 5.5 V,	Outputs open				1	mA
Ci	Control input	V <sub>CC</sub> = 5 V,	V <sub>I</sub> = 2.5 V or 0.5 V			6.5		pF
	A port		V <sub>O</sub> = 2.5 V or 0.5 V			10		
Cio	B port, PARITY	V <sub>CC</sub> = 5 V,				14		pF
Co	ERR	V <sub>CC</sub> = 5 V,	V <sub>O</sub> = 2.5 V or 0.5 V			10		рF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. <sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current. § Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



# SN74BCT657 OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SCBS079B - NOVEMBER 1991 - REVISED APRIL 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Note 3)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	МАХ	UNIT
	(INPUT)	(001F01)	MIN	TYP	MAX			
<sup>t</sup> PLH	A or B	B or A	1.1	3.1	6	1.1	6.6	00
<sup>t</sup> PHL	AUD	BUIA	2	5.3	8.5	2	9	ns
<sup>t</sup> PLH	А	PARITY	3	7.4	12.7	3	15.4	ns
<sup>t</sup> PHL	А		4.6	8.6	14.1	4.6	15.9	
<sup>t</sup> PLH	ODD/EVEN		1.1	4.1	6.4	1.1	7.1	
<sup>t</sup> PHL		PARITY, ERR	2.6	5.5	8.3	2.6	9	ns
<sup>t</sup> PLH	В	ERR	3.1	7.4	12.6	3.1	15.3	ns
<sup>t</sup> PHL		EKK	4.4	6.5	13.3	4.4	15.5	115
<sup>t</sup> PLH	PARITY	ERR	3.4	7.7	10.7	3.4	13.2	ns
<sup>t</sup> PHL		EKK	5.5	8.8	12	5.5	13.9	115
<sup>t</sup> PZH	ŌĒ		1.8	5.1	7.7	1.8	9.1	50
<sup>t</sup> PZL		A, B, PARITY, or ERR	3.2	6.7	14.2	3.2	16.3	ns
<sup>t</sup> PHZ	ŌE	A, B, PARITY, or ERR	2.6	5.7	8	2.6	9.1	
<sup>t</sup> PLZ		A, D, I ANIT I, OI ERR	2	5	7.4	2	8	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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