

# SN54BCT29826, SN74BCT29826 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS076A – NOVEMBER 1991 – REVISED NOVEMBER 1993

- **State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **3-State Inverting Buffer-Type Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)**

## description

These 8-bit bus-interface flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

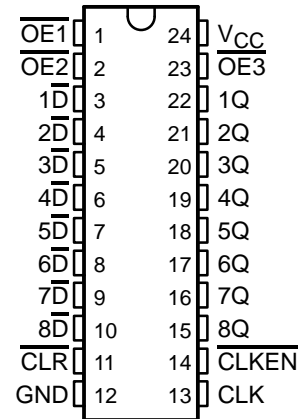
The eight flip-flops are edge-triggered D-type flip-flops. With the clock-enable ( $\overline{CLKEN}$ ) input low, the device enters data on the low-to-high transition of the clock. Taking  $\overline{CLKEN}$  high disables the clock buffer, thus latching the outputs. Taking the clear ( $\overline{CLR}$ ) input low causes the eight Q outputs to go low independently of the clock.

Buffered output-enable ( $\overline{OE1}$ ,  $\overline{OE2}$ , or  $\overline{OE3}$ ) inputs can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

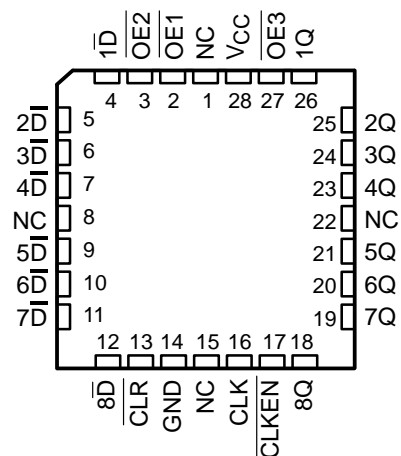
The output-enable inputs do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54BCT29826 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74BCT29826 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54BCT29826 . . . JT OR W PACKAGE  
SN74BCT29826 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54BCT29826 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

# SN54BCT29826, SN74BCT29826

## 8-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCBS076A – NOVEMBER 1991 – REVISED NOVEMBER 1993

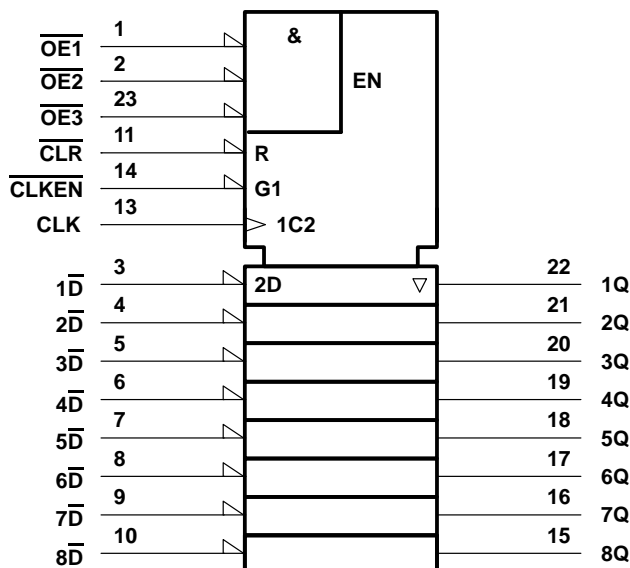
FUNCTION TABLE

INPUTS					OUTPUT Q
$\overline{OE}^\dagger$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	H or L	X	$Q_0$
H	X	X	X	X	Z

$^\dagger \overline{OE}$  = H if any of the output-enable inputs is high.

$\overline{OE}$  = L if all of the output-enable inputs are low.

logic symbol $^\ddagger$



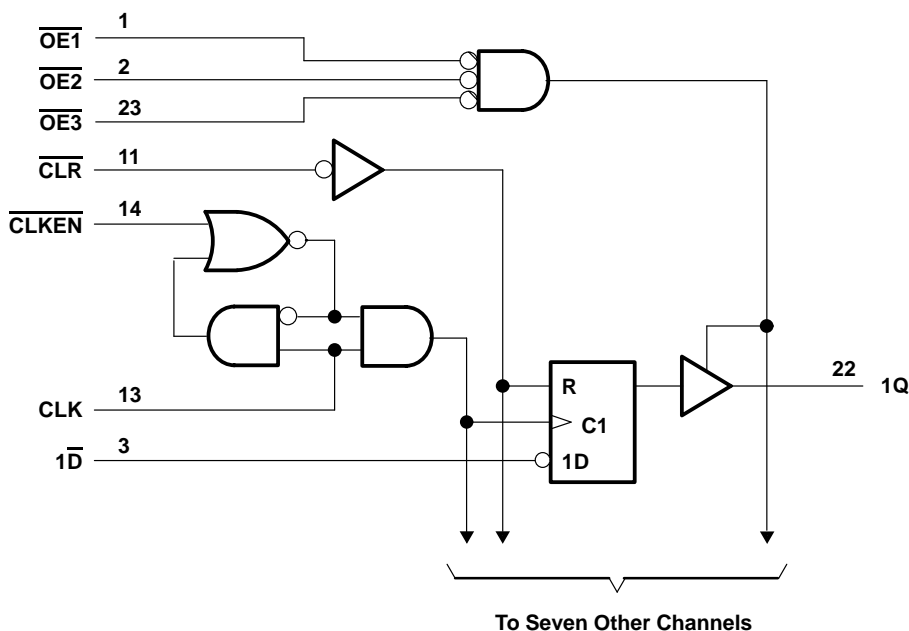
$^\ddagger$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, NT, and W packages.

# SN54BCT29826, SN74BCT29826 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS076A – NOVEMBER 1991 – REVISED NOVEMBER 1993

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–30 mA
Current into any output in the low state, $I_O$ : SN54BCT29826	48 mA
SN74BCT29826	96 mA
Operating free-air temperature range: SN54BCT29826	–55°C to 125°C
SN74BCT29826	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## recommended operating conditions

		SN54BCT29826			SN74BCT29826			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–15			–24	mA
$I_{OL}$	Low-level output current			24			48	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54BCT29826, SN74BCT29826

## 8-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCBS076A – NOVEMBER 1991 – REVISED NOVEMBER 1993

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54BCT29826			SN74BCT29826			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -15\text{ mA}$	2	3.2		2.4	3.3		V
		$I_{OH} = -24\text{ mA}$				2	3.1		
	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3\text{ mA}$				2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 24\text{ mA}$		0.38	0.55				V
		$I_{OL} = 48\text{ mA}$				0.42	0.55		
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$	-10		-75	-10		-75	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-0.2			-0.2	mA
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-75		-250	-75		-250	mA
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			20			20	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$			-20			-20	$\mu\text{A}$
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open	26		40	26		40	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open	10		15	10		15	mA
$I_{CCZ}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open	6		10	6		10	mA
$C_i$	$V_{CC} = 5\text{ V}$ ,	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$		5			5		pF
$C_o$	$V_{CC} = 5\text{ V}$ ,	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$		7			7		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

			$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54BCT29826		SN74BCT29826		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		0	125	0	125	0	125	MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	5		5		5		ns
		CLK high or low	4		4		4		
$t_{\text{su}}$	Setup time before $\text{CLK}\uparrow$	Data high	3		3		3		ns
		Data low	6		6		6		
		$\overline{\text{CLR}}$	1		1		1		
		$\overline{\text{CLKEN}}$ high	6		6		6		
		$\overline{\text{CLKEN}}$ low	7		7		7		
$t_h$	Hold time after $\text{CLK}\uparrow$	Data high	0.5		0.5		0.5		ns
		Data low	1.5		1.5		1.5		
		$\overline{\text{CLKEN}}$ high or low	1		1		1		



**SN54BCT29826, SN74BCT29826**  
**8-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCBS076A – NOVEMBER 1991 – REVISED NOVEMBER 1993

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54BCT29826		SN74BCT29826		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			125			125		125		MHz
$t_{PLH}$	CLK	Q	1.5	5.8	8.1	1.5	10	1.5	9.1	ns
$t_{PHL}$			2.4	6	8	2.4	9.4	2.4	8.6	
$t_{PHL}$	$\overline{\text{CLR}}$	Q	2.2	6.3	8.7	2.2	10	2.2	9.9	ns
$t_{PZH}$	$\overline{\text{OE}}$	Q	1.5	6	8.4	1.5	10.6	1.5	10	ns
$t_{PZL}$			4	8.8	11.3	4	13.4	4	12.9	
$t_{PHZ}$	$\overline{\text{OE}}$	Q	1.6	5.6	7.7	1.6	9.7	1.6	8.9	ns
$t_{PLZ}$			1	4.9	7	1	8.8	1	7.7	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.