

SCBS057G – DECEMBER 1990 – REVISED MAY 1997

- SN54ABT16500B . . . WD PACKAGE
SN74ABT16500B . . . DGG OR DL PACKAGE
(TOP VIEW)

SN54ABT16500B, SN74ABT16500B

18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT16500B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16500B is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0^{\ddagger}
H	L	L	X	B_0^{\S}

† A-to-B data flow is shown: B-to-A flow is similar but uses \overline{OEBA} , \overline{LEBA} , and \overline{CLKBA} .

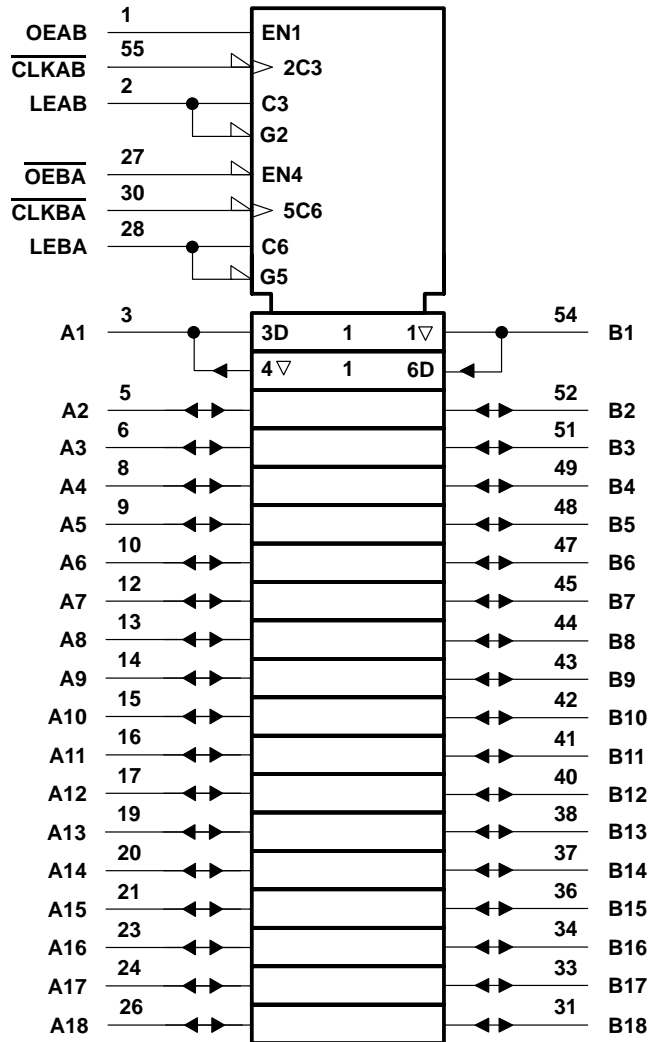
‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

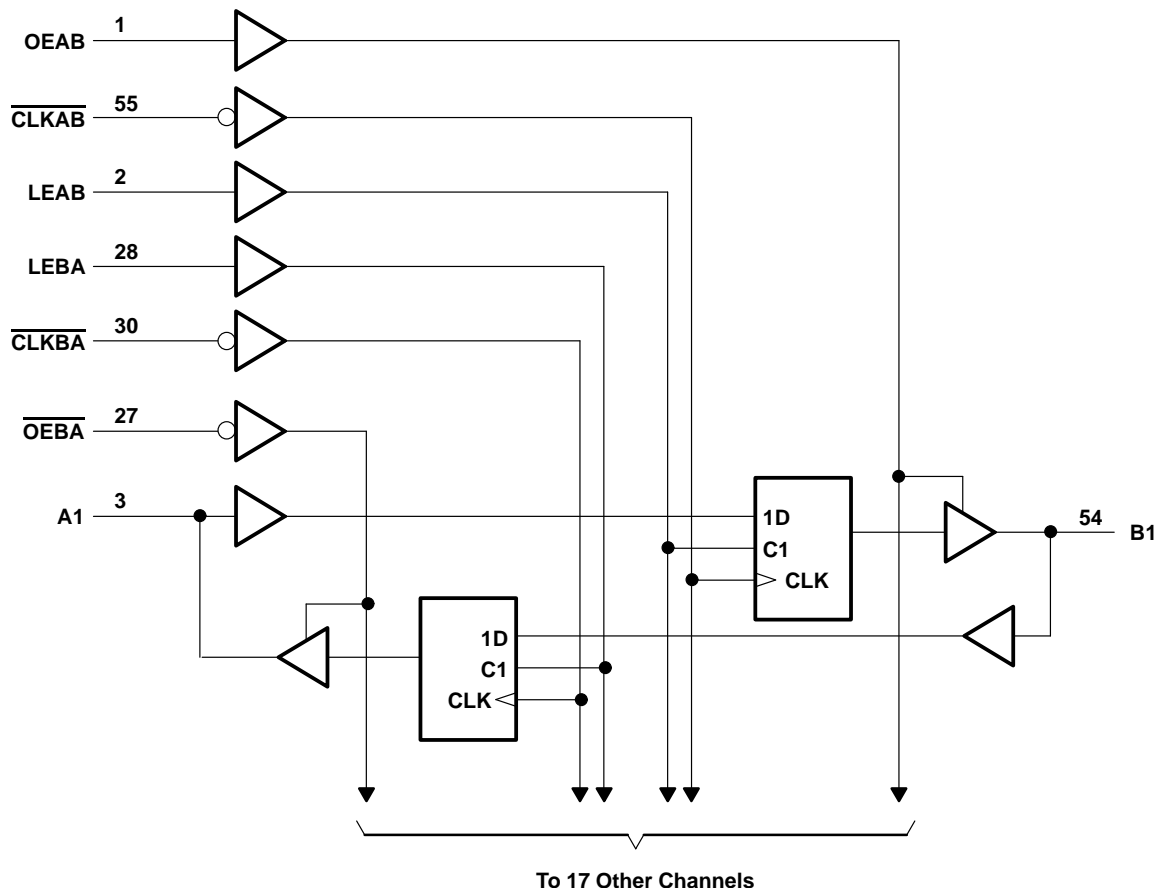
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16500B	96 mA
SN74ABT16500B	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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recommended operating conditions (see Note 3)

			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μ s/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
		V _{CC} = 4.5 V, I _{OH} = -24 mA	2			2				
		V _{CC} = 4.5 V, I _{OH} = -32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 48 mA			0.55		0.55			V
		V _{CC} = 4.5 V, I _{OL} = 64 mA			0.55*				0.55	
V _{hys}				100						mV
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50		50		50	μA
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND			±20		±20		±20	
I _{O†}		V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I _{OZPU} §		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, \overline{OE} or OE = X			±50		±50		±50	μA
I _{OZPD} §		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, \overline{OE} or OE = X			±50		±50		±50	μA
I _{OZH} ¶		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, \overline{OE} ≥ 2 V, OE ≤ 0.8 V#			10		10		10	μA
I _{OZL} ¶		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, \overline{OE} ≥ 2 V, OE ≤ 0.8 V#			-10		-10		-10	μA
I _{CC}	A or B ports	V _{CC} = 5.5 V, Outputs high			3		3		3	mA
		I _O = 0, Outputs low			36		36		36	
		V _I = V _{CC} or GND, Outputs disabled			3		3		3	
ΔI _{CC}		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			50		50		50	μA
C _i	Control inputs	V _I = 2.5 V or 0.5 V			3					pF
C _{iO}	A or B ports	V _O = 2.5 V or 0.5 V			9					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This parameter is characterized, but not production tested.

¶ The parameters I_{OZH} and I_{OZL} include the input leakage current.

For V_{CC} between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

|| This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			0	150	0	150	MHz
t _w [†]	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3		3		
t _{su}	Setup time	A before CLKAB↓		3		3		ns
		B before CLKBA↓		3		3		
		A before LEAB↓ or B before LEBA↓	CLK high	1		1		
			CLK low	2.5		2.5		
t _h	Hold time	A after CLKAB↓ or B after CLKBA↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

† This parameter is characterized, but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150		MHz
t_{PLH}	A or B	B or A	1	2.5	3.6	1	4.2	1	4	ns
t_{PHL}			1	3.2	4.5	1	5.1	1	4.9	
t_{PLH}	LEAB or LEBA	B or A	1	3.2	4.5	1	5.6	1	5	ns
t_{PHL}			1	3.4	4.5	1	5.4	1	5	
t_{PLH}	$\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$	B or A	1	3.5	4.7	1	5.4	1	5.3	ns
t_{PHL}			1	3.5	4.7	1	5.4	1	5.3	
t_{PZH}	OEAB or $\overline{\text{OEBA}}$	B or A	1	3.4	4.6	1	5.3	1	5.1	ns
t_{PZL}			1.5	3.8	4.7	1.5	5.6	1.5	5.4	
t_{PHZ}	OEAB or $\overline{\text{OEBA}}$	B or A	1.5	4.5	5.7	1.5	6.9	1.5	6.5	ns
t_{PLZ}			1.4	3.4	4.7	1.4	5.8	1.4	5.4	

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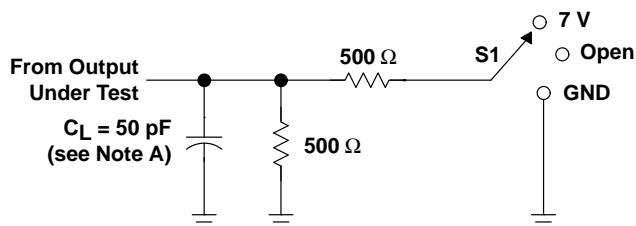
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WITH 3-STATE OUTPUTS

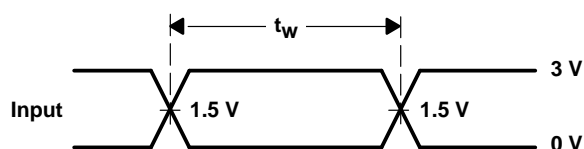
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PARAMETER MEASUREMENT INFORMATION

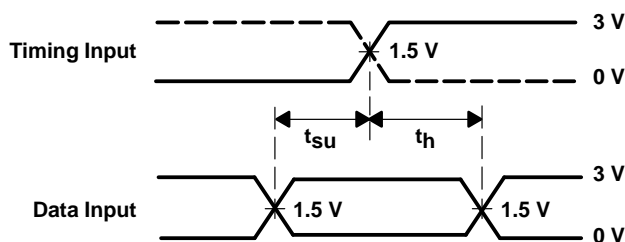


LOAD CIRCUIT

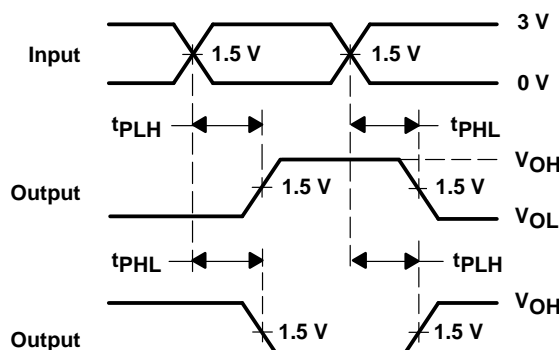
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



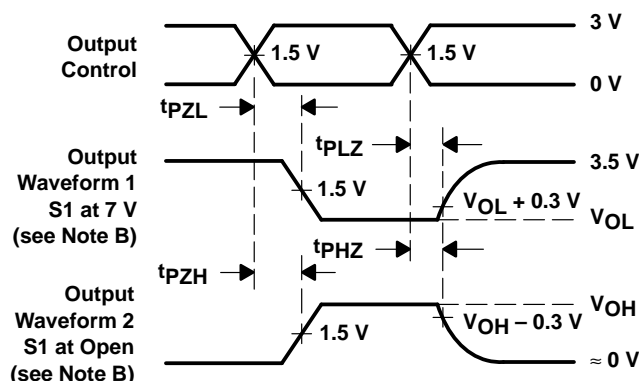
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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