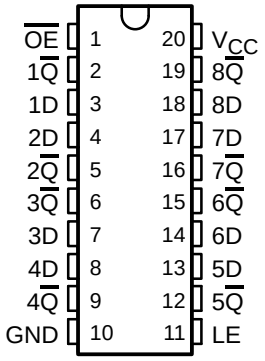
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Full Parallel Access for Loading**
- **3-State Inverting Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-Std-883C, Method 3015**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



description

The SN74BCT533 is an 8-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

When the latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse of the levels set up at the D inputs. The SN74BCT533 provides inverted data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT533 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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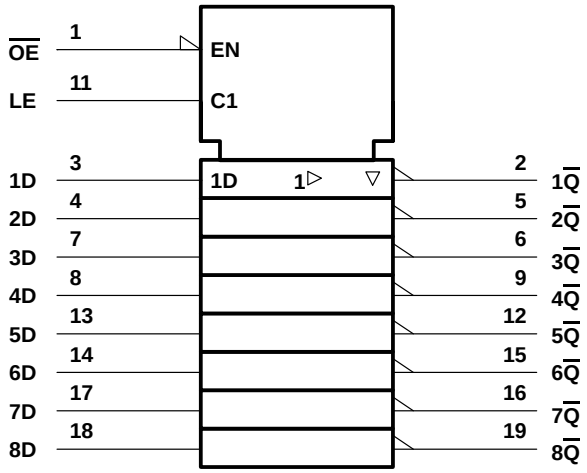
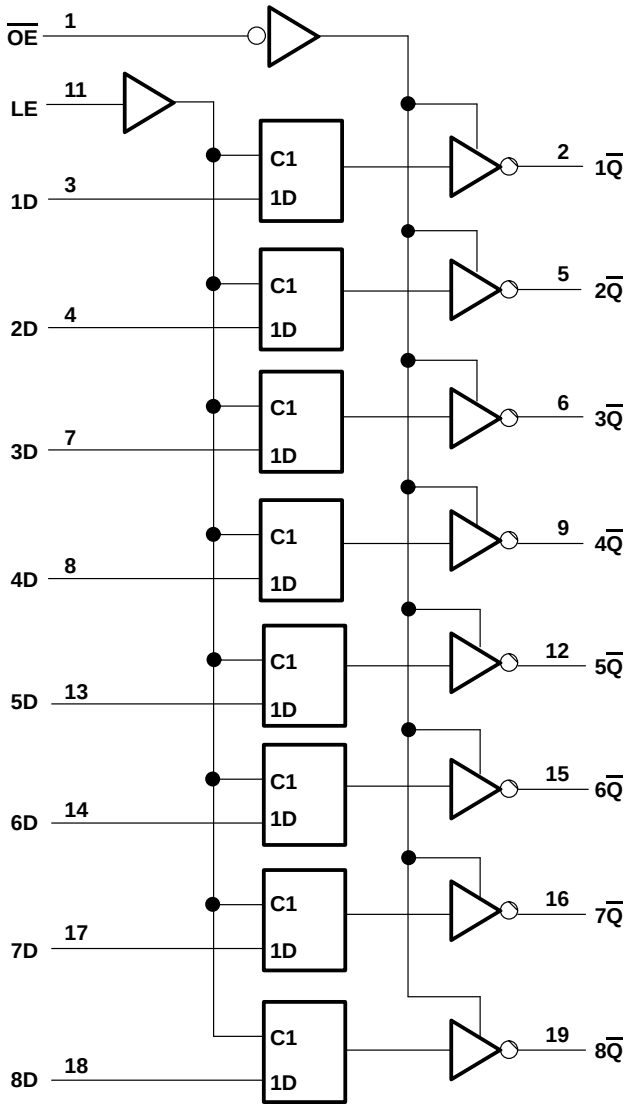
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Input clamp current . . . . . –30 mA
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.3		V
		I_{OH} = –15 mA	2	3.1		
	V_{CC} = 4.75 V,	I_{OH} = –3 mA	2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 64 mA		0.42	0.55	V
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.4	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	–100		–225	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{CCL}	V_{CC} = 5.5 V			40	63	mA
I_{CCH}	V_{CC} = 5.5 V			5	8	mA
I_{CCZ}	V_{CC} = 5.5 V			5	8	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration, LE high		4		4		ns
t_{su}	Setup time, data before LE↓	High or low	2.5		2.5		ns
t_h	Hold time, data after LE↓	High or low	3		3		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	2.8	6.1	9.1	2.8	11.2	ns
t_{PHL}			2.7	5.3	8.2	2.7	9.3	
t_{PLH}	LE	$\overline{Q}$	2.3	5	7.7	2.3	8.6	ns
t_{PHL}			2.5	4.9	7.6	2.5	8.1	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	3.1	6.1	8.8	3.1	10.8	ns
t_{PZL}			3.7	6.9	10	3.7	12	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	1.8	3.9	5.9	1.8	6.9	ns
t_{PLZ}			1.3	3.5	6.1	1.3	7.2	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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