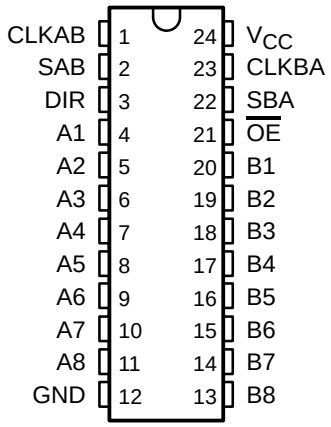
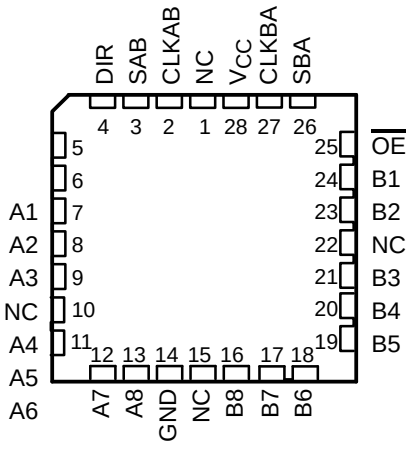
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Power-Up High-Impedance Mode**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPS (JT, NT)**

SN54BCT648 . . . JT OR W PACKAGE
SN74BCT648 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT648 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′BCT648.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select control (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54BCT648 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT648 is characterized for operation from 0°C to 70°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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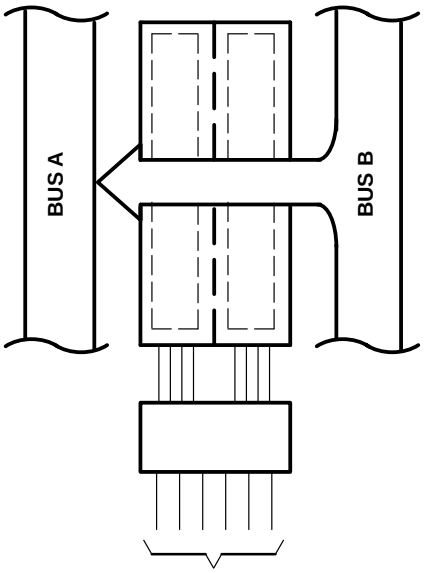
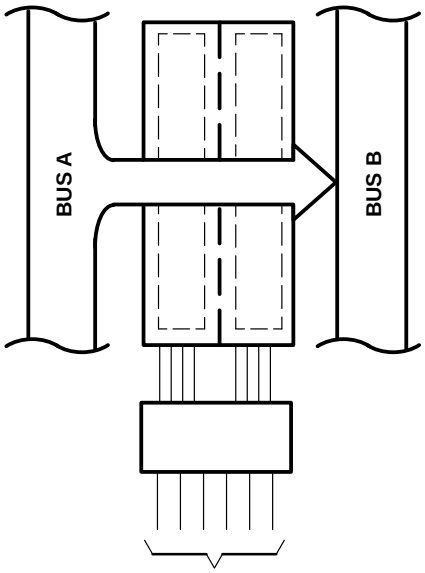


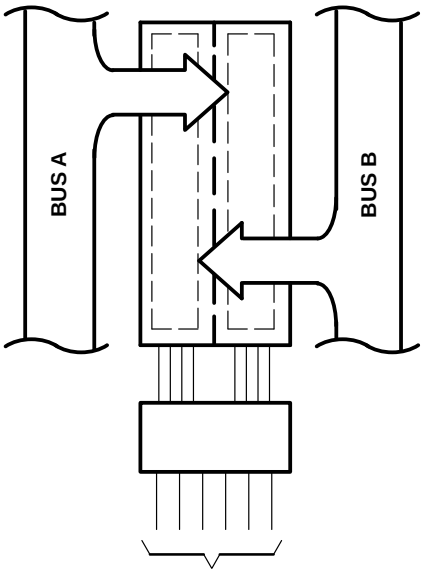
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



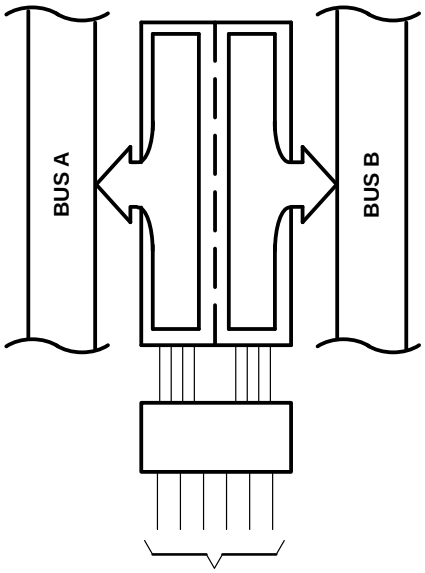
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A OR B

Figure 1. Bus-Management Functions

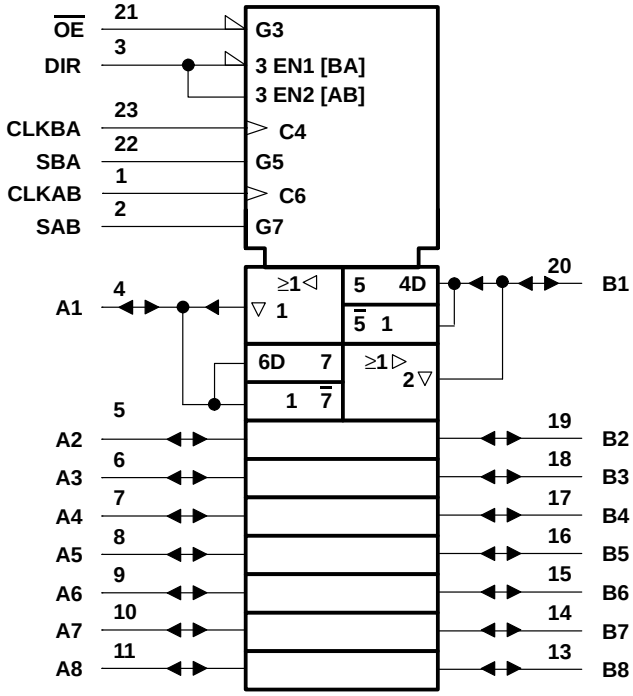
Pin numbers shown are for the DW, JT, NT, and W packages.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ data to A Bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B Bus

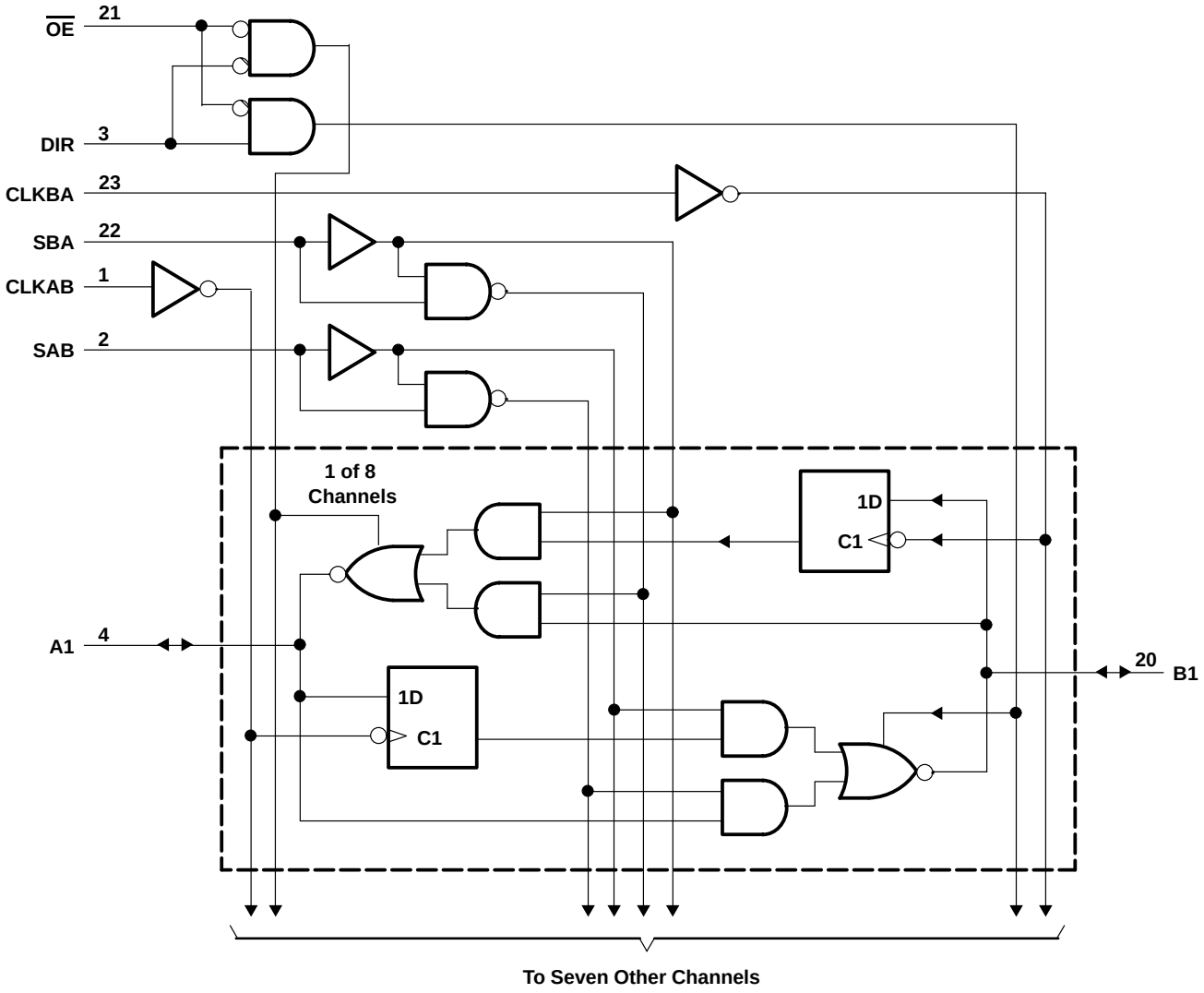
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range (I/O ports) (see Note 1) . . . . . – 0.5 V to 5.5 V
Input voltage range (excluding I/O ports) (see Note 1) . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Current into any output in the low state: SN54BCT648 . . . . . 96 mA
SN74BCT648 . . . . . 128 mA
Operating free-air temperature range: SN54BCT648 . . . . . – 55°C to 125°C
SN74BCT648 . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT648			SN74BCT648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT648			SN74BCT648			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = –12 mA	2	3.2					
			I_{OH} = –15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I	A or B port	V_{CC} = 5.5 V,	V_I = 5.5 V			1			1	mA
	Control inputs					1			1	
I_{IH}‡	A or B port	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	µA
	Control inputs					20			20	
I_{IL}‡	A or B port	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.7			–0.7	mA
	Control inputs					–0.7			–0.7	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	–100		–225	–100		–225	mA
I_{CCL}	A or B port	V_{CC} = 5.5 V,	V_I = GND		42	66		42	66	mA
I_{CCH}	A or B port	V_{CC} = 5.5 V,	V_I = 4.5 V		8	13		8	13	mA
I_{CCZ}	A or B port	V_{CC} = 5.5 V,	V_I = GND		10	16		10	16	mA
C_i	Control inputs	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_{io}	A or B port	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		12			12		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54BCT648		SN74BCT648		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	67	0	67	0	67	MHz
t_w	Pulse duration	CLK high	7.5		4.3		7.5		ns
		CLK low	7.5		7.5		7.5		
t_{su}	Setup time, A or B before CLK↑		6		6		6		ns
t_h	Hold time, A or B after CLK↑		1		1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT648		SN74BCT648		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			67	110		67		67		MHz
t_{PLH}	CLKBA or CLKAB	A or B	3.7	7.4	10.3	3.7	13.4	3.7	12.1	ns
t_{PHL}			4.3	7.8	10.6	4.3	13.2	4.3	12.5	
t_{PLH}	A or B	B or A	3.8	7.4	9.9	3.8	12.8	3.8	12.2	ns
t_{PHL}			3.3	6.5	8.9	3.3	11.2	3.3	10.1	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	3.3	6.2	8.4	3.3	10.7	3.3	9.7	ns
t_{PHL}			5.3	9.6	12.6	5.3	16.5	5.3	15.5	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	4.6	8.8	11.7	4.6	16.5	4.6	14.3	ns
t_{PHL}			4.9	8.4	11.1	4.9	13.8	4.9	13	
t_{PZH}	$\overline{OE}$	A or B	4.5	8.4	11	4.5	14.4	4.5	13.5	ns
t_{PZL}			4.9	9.2	12.2	4.9	16	4.9	15	
t_{PHZ}	$\overline{OE}$	A or B	4	7.3	9.7	4	12	4	11.2	ns
t_{PLZ}			3.5	6.6	9.3	3.5	11.6	3.5	10.5	
t_{PZH}	DIR	A or B	3.1	7.4	11	3.1	14.1	3.1	13.4	ns
t_{PZL}			3.8	8.3	12.2	3.8	15.5	3.8	14.7	
t_{PHZ}	DIR	A or B	4.3	8.3	11.6	3.5	14.3	4.3	13.9	ns
t_{PLZ}			2.7	6.7	9.9	2.7	12.8	2.7	11.9	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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