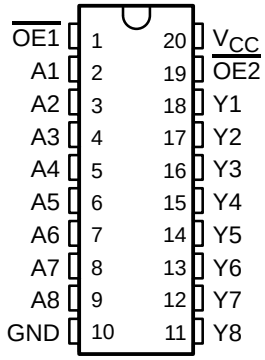
- **BiCMOS Design Significantly Reduces Standby Current**
- **3-State True Outputs Drive Bus Lines or Buffer Memory-Address Registers**
- **High-Impedance State During Power Up and Power Down**
- **P-N-P Inputs Reduce DC Loading**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

The SN64BCT541A octal buffer and line driver is ideal for driving bus lines or buffering memory-address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

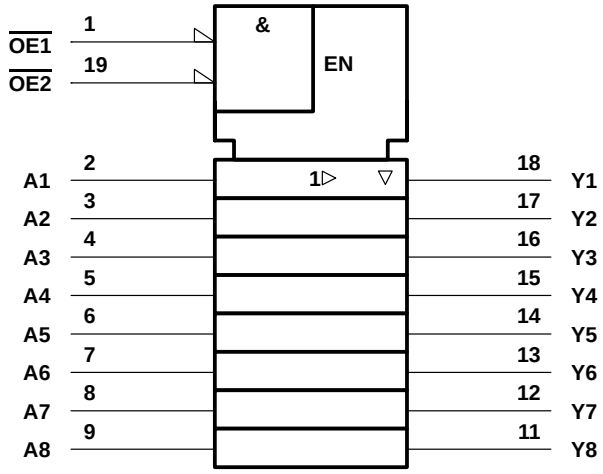
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT541A is characterized for operation from –40°C to 85°C and from 0°C to 70°C.

**FUNCTION TABLE**

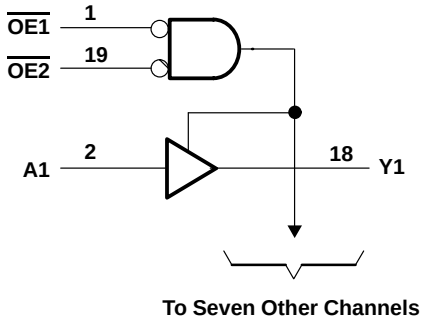
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

### logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ . . . . . –0.5 V to $V_{CC}$
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range, $T_A$ . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

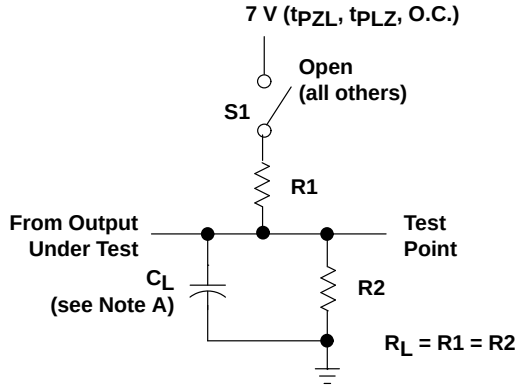
| PARAMETER | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = –15 mA | | 2 | 3.1 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = 64 mA | | | 0.42 | 0.55 | V |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | µA |
| $I_{OZ}$ | $V_{CC}$ = 0 to 2.3 V (power up) | $V_O$ = 2.7 V or 0.5 V, | $\overline{OE}$ at 0.8 V | | | ± 50 | µA |
| | $V_{CC}$ = 1.8 V to 0 (power down) | | | | | ± 50 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | | –0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | –100 | | –225 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V | | | | 47 | 72 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V | | | | 27 | 40 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V | | | | 5 | 7 | mA |
| $C_i$ | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | | 5 | | pF |
| $C_o$ | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | | 10 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

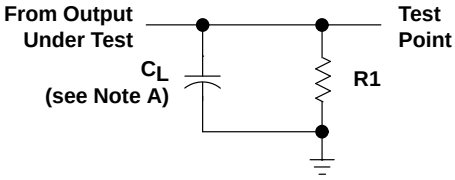
## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$ = –40°C to 85°C | | $T_A$ = 0°C to 70°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 2.1 | 3.7 | 5.3 | 1.7 | 6.3 | 1.7 | 6 | ns |
| $t_{PHL}$ | | | 3.7 | 5.5 | 7.5 | 3.2 | 8.7 | 3.4 | 8.2 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 4.5 | 7.2 | 9.3 | 4.4 | 11 | 3.9 | 10.7 | ns |
| $t_{PZL}$ | | | 5 | 8 | 10.4 | 5.4 | 12.4 | 4.4 | 11.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 3.5 | 5.6 | 7.6 | 3 | 9.1 | 3 | 8.6 | ns |
| $t_{PLZ}$ | | | 3.9 | 5.2 | 7.2 | 3 | 9.4 | 3 | 8.6 | |

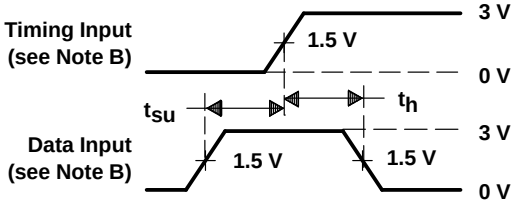
## PARAMETER MEASUREMENT INFORMATION



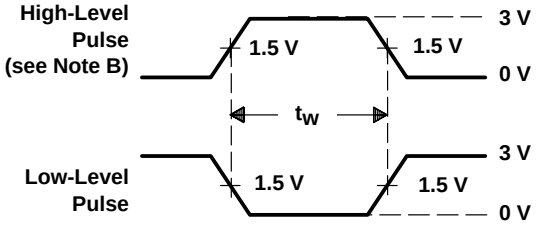

**LOAD CIRCUIT FOR**
**3-STATE AND OPEN-COLLECTOR OUTPUTS**



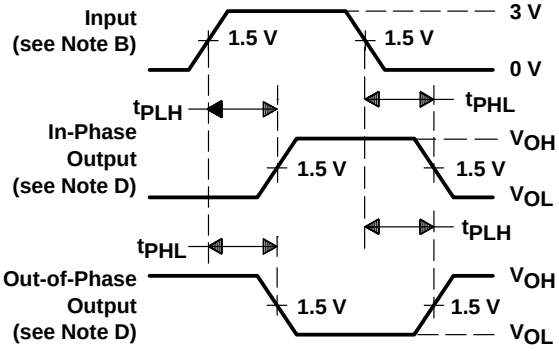

**LOAD CIRCUIT FOR**
**TOTEM-POLE OUTPUTS**



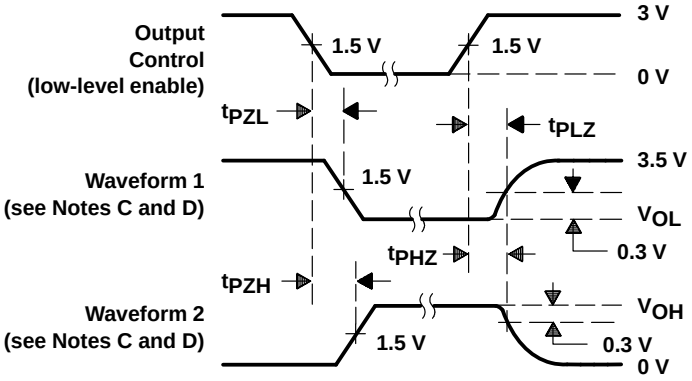

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**




**VOLTAGE WAVEFORMS**
**PULSE DURATION**




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES (see Note D)**




**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

**Figure 1. Load Circuits and Voltage Waveforms**

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