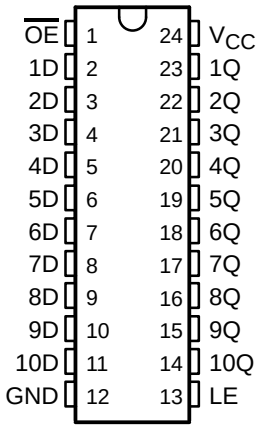
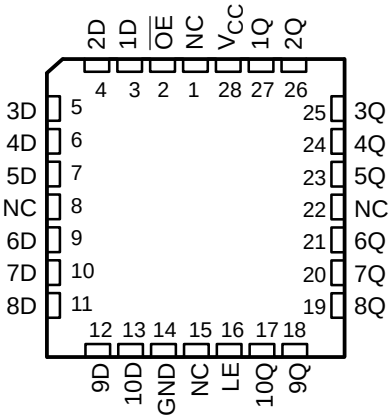
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Power-Up High-Impedance State**
- **Provides Extra Bus-Driving Latches Necessary For Wider Address/Data Paths or Buses With Parity**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)**

SN54BCT29841 . . . JT OR W PACKAGE
SN74BCT29841 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT29841 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 10-bit bus-interface latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten latches of the ′BCT29841 are transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{OE}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54BCT29841 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT29841 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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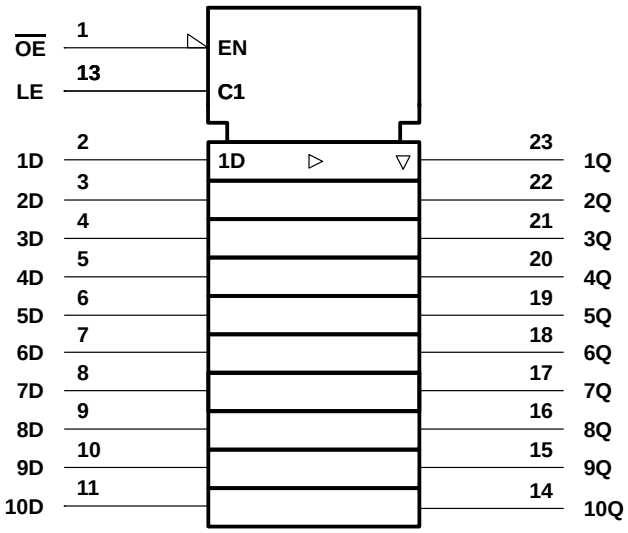
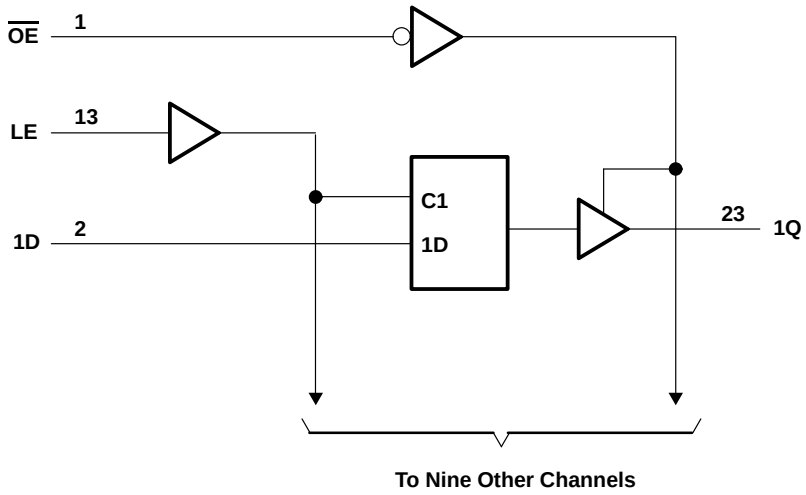
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . –30 mA
Current into any output in the low state, I_O: SN54BCT29841 . . . . . 48 mA
SN74BCT29841 . . . . . 96 mA
Operating free-air temperature range: SN54BCT29841 . . . . . – 55°C to 125°C
SN74BCT29841 . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		SN54BCT29841			SN74BCT29841			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–15			–24	mA
I_{OL}	Low-level output current			24			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT29841			SN74BCT29841			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –15 mA	2.4			2.4			V
		I_{OH} = –24 mA				2			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 24 mA		0.35	0.55				V
		I_{OL} = 48 mA					0.42	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V	–10		–75	–10		–75	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.2			–0.2	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	–75		–275	–75		–275	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–20			–20	µA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		3	7		3	7	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		24	35		24	35	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		3	7		3	7	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5.5			5.5		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		8			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54BCT29841		SN74BCT29841		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low		4		4		4		ns
t_{su}	Setup time, data before LE↓		2		2		2		ns
t_h	Hold time, data after LE↓	High	1.5		1.5		1.5		ns
		Low	3.5		3.5		3.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT29841		SN74BCT29841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.8	4.7	6.7	1.8	8.1	1.8	7.5	ns
t_{PHL}			2	5	7.3	2	9.1	2	8.6	
t_{PLH}	LE	Q	2.5	5.4	7.6	2.5	9.3	2.5	8.6	ns
t_{PHL}			2.7	5.4	7.5	2.7	8.7	2.7	8.1	
t_{PZH}	$\overline{OE}$	Q	1.8	5.3	7.4	1.8	9.2	1.8	9.2	ns
t_{PZL}			4.4	8.1	10.6	4.4	13.4	4.4	12.8	
t_{PHZ}	$\overline{OE}$	Q	2.6	4.9	6.9	2.6	7.7	2.6	6.9	ns
t_{PLZ}			1.6	4.4	6.3	1.6	7.7	1.6	6.9	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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