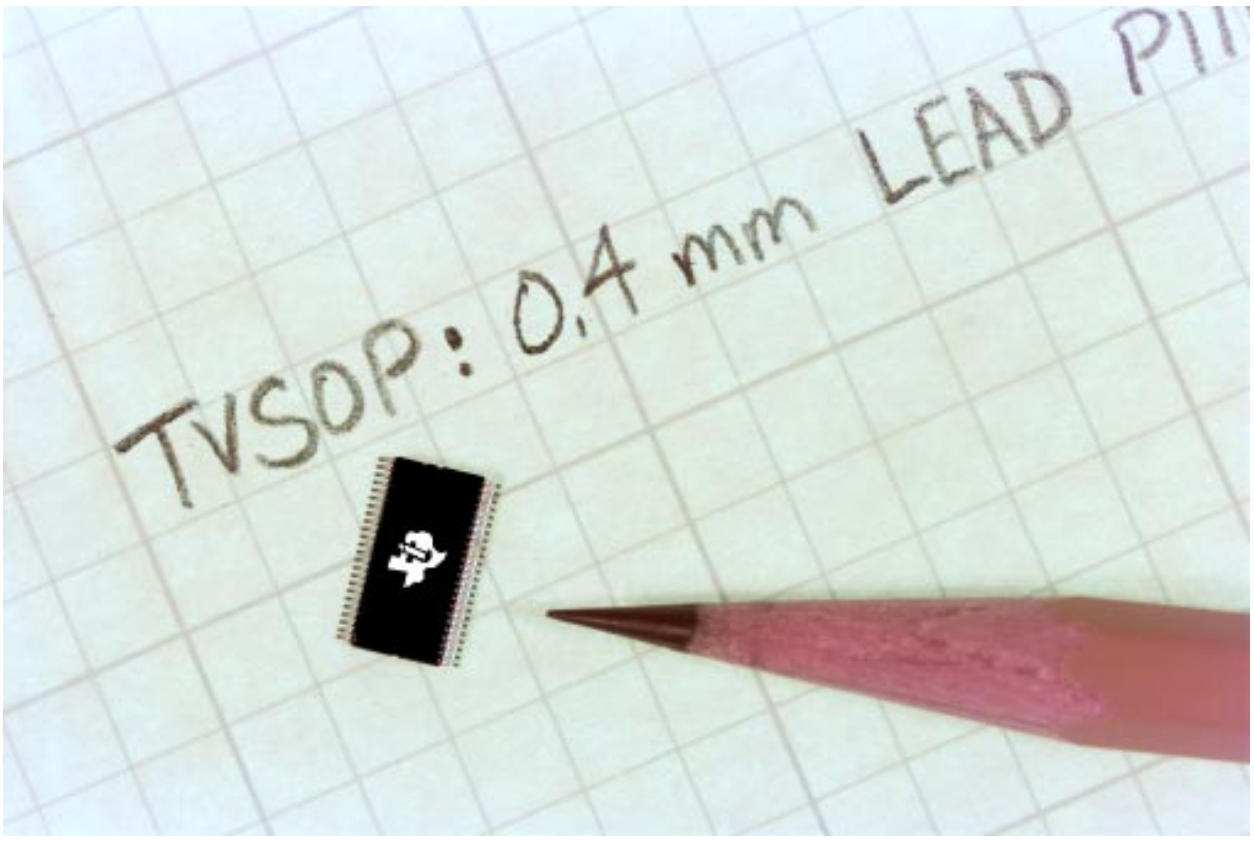
TEXAS INSTRUMENTS

TVSOP Application Brief



August 1996 (draft 1.2) SCBA009A

The Thin Very Small Outline Package (TVSOP)

Acknowledgment

The authors wish to acknowledge the following persons and corporations for their invaluable assistance in the preparation of this document.

Our co-workers in Advanced System Logic (ASL) and the Dallas Process Automation Center (DPAC) provided expert technical and editorial help and guidance. Without their support, this report would not have been possible.

Advanced System Logic, Texas Instruments, Sherman, TX
- David Holmgreen, ASL Launch Marketing
- Douglas Romm, ASL Packaging, (Thermal Modeling)
- Cles Troxtell, ASL Test Finish

AVEX Electronics, Incorporated, a subsidiary of J.M. Huber Corporation, Huntsville, AL

Process Automation Center, Texas Instruments, Dallas, TX
- Darvin Edwards
- Mike Lamson

Solectron, Texas (formerly Custom Manufacturing Services, Texas Instruments), Austin, TX
- David M. Mendez
- Glen C. Shepherd
- David M. Spitz
- George C. Zbranek, Jr.

June 1996

Maria Y. Balian
Edgar Zuniga-Ortiz
ASL New Package Development

Table of Contents

List of Tables

List of Figures

List of Equations

Introduction

Development of portable, light-weight, high-performance electronics products is driving the semiconductor industry toward smaller, thinner and higher-density packages. Pricing pressures are encouraging strong efforts toward cost reduction.

Texas Instruments has always been a leader in IC packaging and is now introducing a new family of Thin Very Small Outline Packages (TVSOP) to support the component miniaturization requirements of the industry. The new TVSOP package family, in 14, 16, 20, 24, 48, 56, 80 and 100-pin types, features a lead pitch of 0.4 mm (16 mil.) and a device height meeting the 1.2 mm PCMCIA (Personal Computer Memory Card International Association) requirement. The TVSOP packages have received JEDEC (Joint Electronics Device Engineering Council) registration under semiconductor package standard MO-194.

In this application article, we provide an overview of the TVSOP package family characteristics including thermal, electrical, reliability and moisture sensitivity performance. Assembly and mounting guidelines for devices in 0.4 mm lead pitch packages are also included.

TVSOP Dimensions

Figure 1 and Table 1 show TVSOP package dimensions.

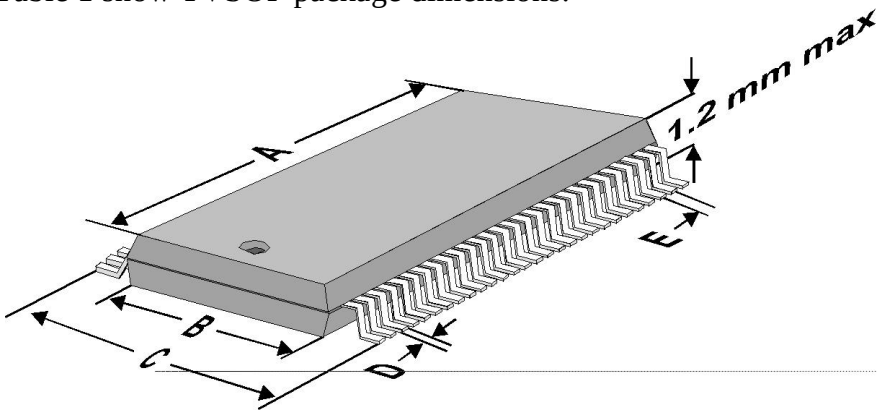


Figure 1: TVSOP Dimensions

TVSOP Package	Typical Dimensions (in mm)					Area (mm^2)	% Smaller than SSOP	% Smaller than TSSOP	% Smaller than TQFP
	A	B	C	D	E				
14-Pin	3.60	4.40	6.40	0.18	0.40	23.00	52.4	29.3	
16-Pin	3.60	4.40	6.40	0.18	0.40	23.00	52.4	29.3	
20-Pin	5.00	4.40	6.40	0.18	0.40	32.00	43.0	24.0	
24-Pin	5.00	4.40	6.40	0.18	0.40	32.00	50.0	34.0	
48-Pin	9.80	4.40	6.40	0.18	0.40	63.00	61.9	38.0	
56-Pin	11.3	4.40	6.40	0.18	0.40	72.30	62.2	36.0	
80-Pin	17.0	6.10	8.10	0.18	0.40	137.8			30.0
100-Pin	20.8	6.10	8.10	0.18	0.40	168.5			35.0

Table 1: TVSOP Dimensions by Pin Count

Advanced System Logic (ASL) Packaging Trends

Figure 2 shows how the TVSOP package follows the trend toward smaller and smaller surface mount packages.

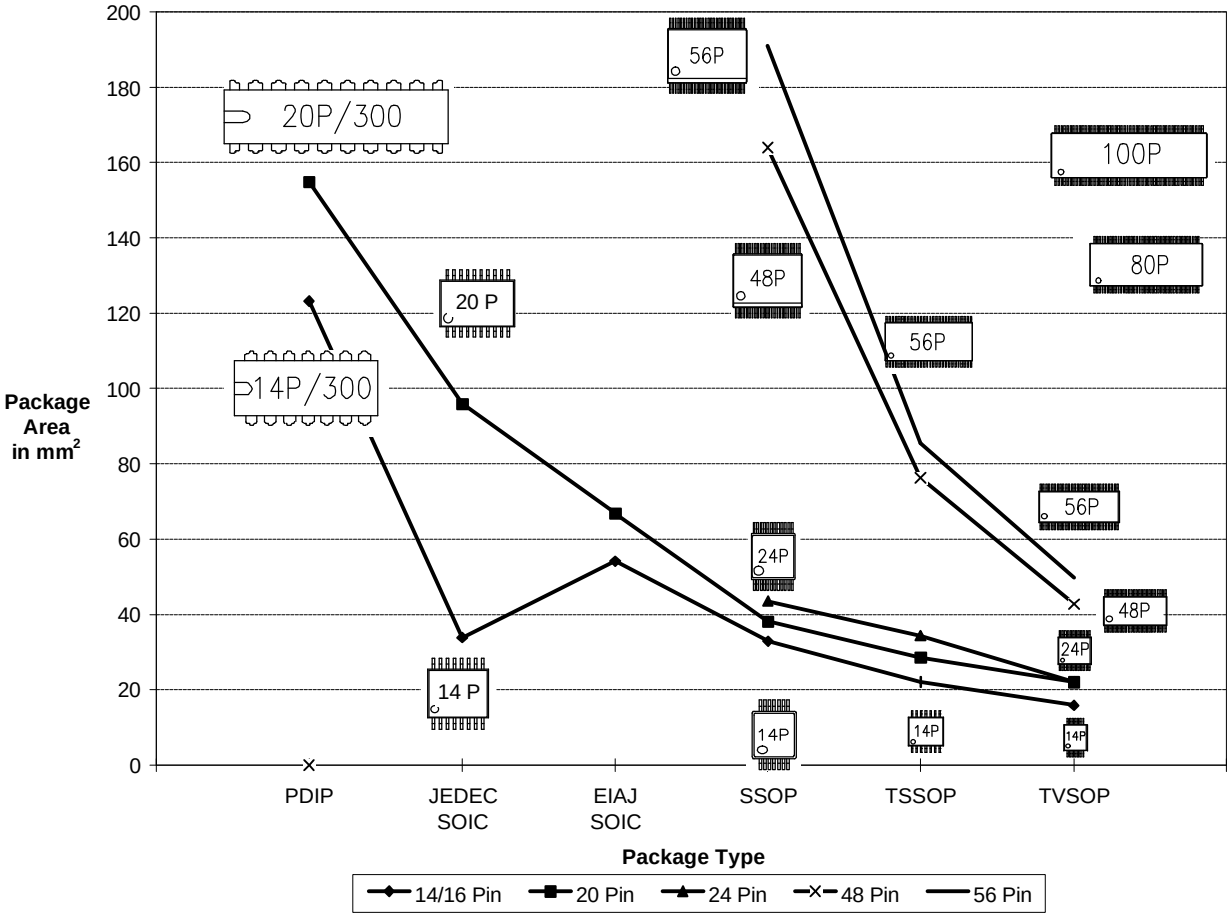
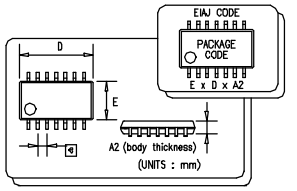


Figure 2: Package Area Comparison

ASL Line-Up of Similar Packages

Figure 3 illustrates Texas Instruments SSOP, TSSOP and TVSOP surface mount packages with pin pitches of 0.65 to 0.40 mm.

PACKAGE TYPE	EIAJ Type (mil)	PITCH e	14	16	20	24	48	56	100	80	JEDEC
SSOP	II 300	0.65	DB 5.3 x 6.2 x 1.8	DB 5.3 x 6.2 x 1.8	DB 5.3 x 7.2 x 1.8	DB 5.3 x 8.2 x 1.8					
	III 375	0.635					DL 7.5 x 15.9 x 2.3	DL 7.5x 18.4 x 2.3			
TSSOP	I 225	0.65	PW 4.4 x 5.0 x 1.0	PW 4.4 x 5.0 x 1.0	PW 4.4 x 6.5 x 1.0	PW 4.4 x 7.8 x 1.0					MO-153
	II 300	0.50					DGG 6.1 x 12.5 x 1.0	DGG 6.1 x 14.0 x 1.0			MO-153
TVSOP	I 225	0.40	DGV 4.4 x 3.6 x 1.0	DGV 4.4 x 3.6 x 1.0	DGV 4.4 x 5.0 x 1.0	DGV 4.4 x 5.0 x 1.0	DGV 4.4 x 9.7 x 1.0	DGV 4.4 x 11.3 x 1.0			MO-194
	II 300	0.40							DBB 6.1 x 17.0 x 1.0	DBB 6.1 x 20.8 x 1.0	MO-194

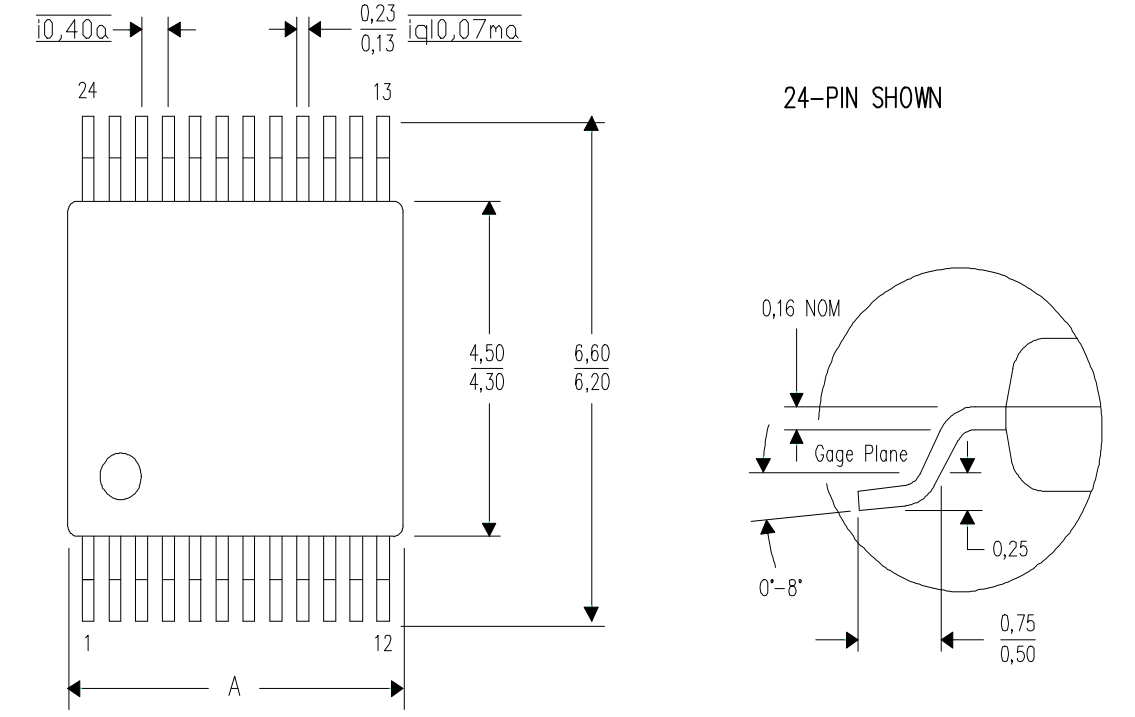
Note: The drawings above are representative only and are not to scale.

Figure 3: SSOP / TSSOP / TVSOP Package Line Up

The TVSOP Package and Its Development

Description

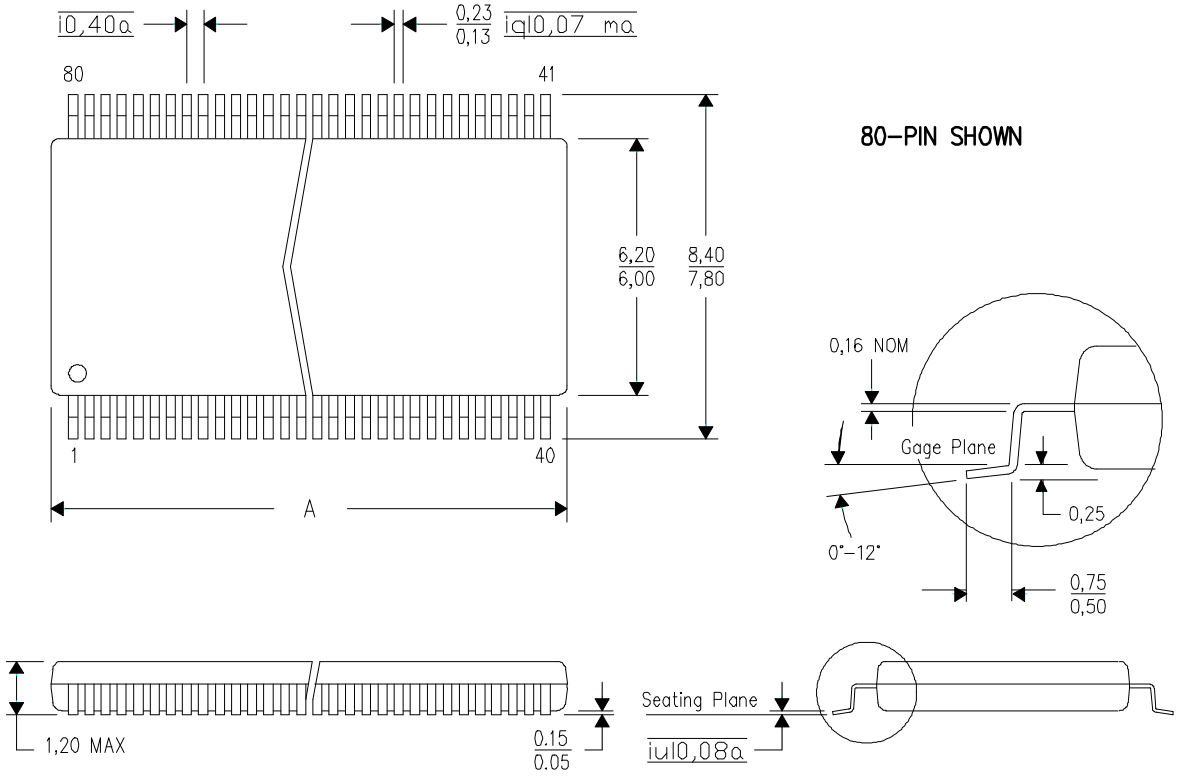
Figures 4 and 5 show the basic dimensions for the TVSOP package.



PINS / DIM	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

Figure 4: 14 to 56-pin TVSOP Package Dimensions



DIM \ PINS	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

Figure 5: 80 and 100-pin TVSOP Package Dimensions

JEDEC Registration

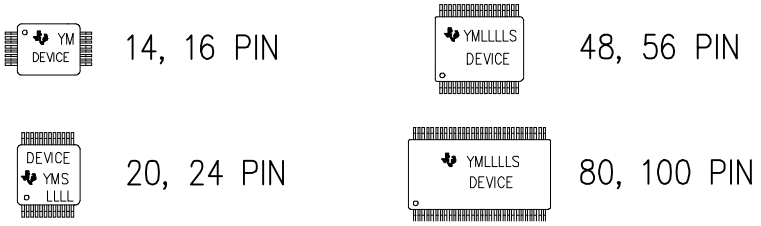
The TVSOP packages have been registered under the JEDEC MO-194 standard for semiconductor packages:

Package	Pins	JEDEC Registration
DGV	14	MO-194AA
DGV	16	MO-194AB
DGV	20	MO-194AC
DGV	24	MO-194AD
DGV	48	MO-194AE
DGV	56	MO-194AF
DBB	80	MO-194BA
DBB	100	MO-194BB

Table 2: JEDEC Registration for TVSOP Packages

Symbolization

Symbolization for the TVSOP follows the Texas Instruments standard. Due to the small size of many of the packages, some characters are omitted or characters substituted for whole part types. Figure 6 shows the general symbol format and Table 3 lists the character omissions or substitutions. The 14 and 16-pin devices are too small to permit the entire Lot Trace Code to be symbolized, only the year of the decade and month characters are included. Complete Lot Trace Code information is included on the product packaging labels.



Y - Year; M - Month; LLLL - Lot Trace Code; S - Site

Figure 6: Product Symbolization Format

Package Type Pin Count	DGV 14,16,20,24	DGV 48,56	DBB 80,100
SN74ALVCH16xxx	N/A	VHxxx	ALVCH16xxx
SN74ALVCHG16xxx	N/A	VGxxx	ALVCHG16xxx
SN74ABTxxx	ABxxx	N/A	N/A
SN74ABTHxxx	AKxxx	N/A	N/A
SN74ABT16xxx	N/A	AHxxx	N/A
SN74ABTH16xxx	N/A	AMxxx	N/A
SN74AHCxxx	HAxxx	N/A	N/A
SN74AHCTxxx	HBxxx	N/A	N/A
SN74CBTD3xxx	CCxxx	N/A	N/A
SN74CBT16xxx	N/A	CYxxx	CBT16xxx
SN74LVCxxx	LCxxx	N/A	N/A
SN74LVCHxxx	LCHxxx	N/A	N/A
SN74LVC16xxx	N/A	LDxxx	N/A
SN74LVCH16xxx	N/A	LDHxxx	N/A

Note: Please contact your nearest TI Sales Office or Authorized Distributor for specific device type availability

Table 3: Product Symbolization

Printed Circuit Board Manufacture with the TVSOP

Overview of Test Site Results

ASL Packaging Engineering has been working in cooperation with Solectron, Texas (formerly TI, Custom Manufacturing Services, Austin) and AVEX Electronics Inc. to develop printed circuit board (PCB) assembly process guidelines for ultra-fine pitch packages in high-volume manufacturing.

The majority of defects encountered in board assembly with fine-pitch packages are caused by solder bridging, open circuits or improper device placement. Proper lead planarity and the absence of bent leads are essential to minimize assembly mount defects. Components with poor co-planarity require more solder paste to obtain a good solder joint. The increased volume of solder paste can in turn cause bridging. All board mounted components must be carefully selected based on the lead foot specifications provided by component suppliers. Lead co-planarity data are constantly monitored on TI TVSOP packages to ensure that all units fall within the JEDEC co-planarity specifications of less than 0.08 mm. Inaccurate device placement, the last of the defect issues, is a function of pick-and-place equipment capability.

Two major potential applications for TVSOP 0.4 mm packages were addressed during the assembly process development project: standard PCB boards (8” x 16”) and standard PCMCIA cards. Many factors can affect the board performance (equipment, environment, component and board quality, etc.), therefore, the guidelines presented herein are primarily intended to give manufacturers and designers useful information that resulted from the lessons learned during our package development work.

TVSOP Results from TI Custom Manufacturing Services (Now Solectron, Texas)

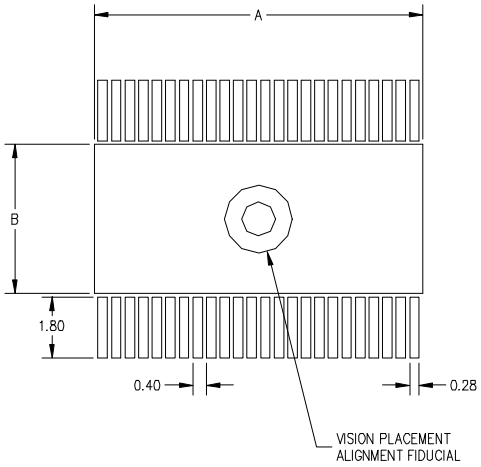
Dave Mendez
Glen Shepherd
Dave Spitz
George Zbranek

Texas Instruments has conducted evaluations to establish the design and processing requirements along with the limitation in applying the TVSOP series of 16 mil (0.4 mm) pitch devices. The intent of this publication is to offer footprint geometry, stencil, placement and SMT processing guidelines. These guidelines are needed to minimize the solder defect rate of indiscriminate use of 16 mil pitch devices in designs.

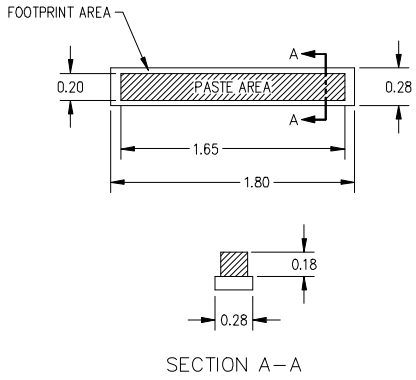
Each SMT assembly process defect rate will be unique to the demands the 16 mil pitch devices will place on the assembly process. Equipment accuracy, repeatability and process capability all play a large role in the resultant defect rate. Therefore we have tried to quantify the differences in magnitude of the rates achievable through implementation of the recommended guidelines.

Pad Geometry Requirements

TVSOP FOOTPRINT



TVSOP STENCIL



See Table below for dimensions A and B

All Dimensions in mm

Pin Count	14 / 16	20 / 24	48	56	80	100
Dimension A	3.6	5.0	9.8	11.3	17.0	20.8
Dimension B	4.4	4.4	4.4	4.4	6.1	6.1

Figure 7: Pad and Stencil Geometry

We recommend 16 mil pitch terminal pad to the following dimensional requirements:

Terminal Pad Length	0.070” (1.8 mm)
Terminal Pad Width	0.011” (0.28 mm)
Terminal Pad Pitch	0.0157” (0.4 mm)
Gerber Tru Position	2 - 4 format minimum
Pad Finish	Entek™

Conclusion The pad geometry and finish are very important to the assembly defect rate for widely spaced 16 mil pitch devices.

Stencil Geometry Requirements

We recommend a single level, laser cut, electro-polished stainless steel 0.006” thick stencil for any product which has both PLCC and 16 mil pitch devices. Boards without PLCC devices could use a 0.005” mil stencil, however, the other 50 mil pitch devices will trend toward insufficient solder volume.

	PLCC and TVSOP	TVSOP ONLY
Stencil Opening Length	0.065”	0.065”
Stencil Opening Width	0.008”	0.008”
Stencil Thickness	0.006”	0.005”
Gerber 7 position	2 - 4 Format minimum	

Conclusion The stencil thickness has the largest influence over the defect rate. Our experience shows that a small increase in the solder short defect rate on 16 mil pitch devices is much better than using a thinner stencil resulting in difficult to detect opens or solder insufficiencies.

Component Placement

All 16 mil pitch device defect rates (shorts) are very sensitive to their lead orientation with respect to the radial distance they reside from the stencil alignment point (usually the center of the board). Widely spaced TVSOP device defect rates can be reduced by orders of magnitude by just placing the device with its leads parallel to the raw PWB image stretch axis. Every board and stencil will have an image positional accuracy which usually manifests itself in an inches per inch mis-registration. Secondly, stencils have an image registration accuracy and tend to change dimensionally with print cycles.

Placement of TVSOP Devices (16 mil devices with lead on 2 sides of the body)

The above dimensional considerations yield the following optimum placement practices. This information applies to any pin count of a 16 mil pitch SOP.

Maximum assembly yields for components placed more than 8 inches away from the center of the board (stencil alignment point) can be achieved by orienting the leads parallel to the board expansion axis with the longest distance from the center point. In areas where the distance from the alignment is excessive (yield degradation area) the defect rate will climb rapidly without special placement guidelines.

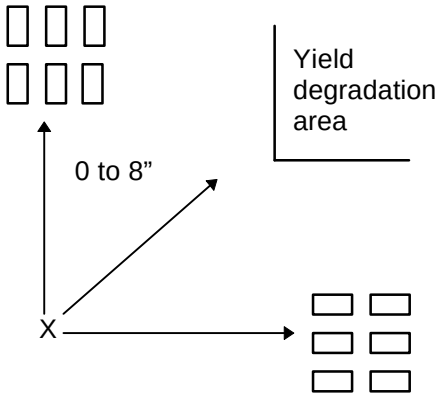


Figure 8: TVSOP Placement on Printed Circuit Boards

Devices outside the 8 inch area must have their lead positioned per Figure 8 or assembly yields will degrade significantly.

Correctly oriented defect expectations (see Figure 8).

Inches from center	1	2	3	4	5	6	7	8	9	10	11
Yield degradation	0	0	0	0	0	0	1x	2x	4x	10x	30x

Note: Magnitude of 4x denotes 4 times the defect rate.

Devices in the yield degradation area of Figure 8 should be avoided. If unavoidable, the leads should be oriented at 45 degrees to the board expansion axis to avoid excessive defects.

Quad Flat Pack (QFP) Devices

This information applies to any pin count 16 mil pitch quad flat pack (leads out all sides) devices.

The QFP device can not avoid defects by orienting their leads at 0 to 90 degrees. Secondly there is the added complication of the stenciling inconsistency with leads in both directions.

The optimum assembly yields of a QFP device are realized when the component is rotated at 45 degrees to the board expansion axis. Significant defects were experienced at all distances more than 4 inches away from the stencil alignment point with normally oriented QFP.

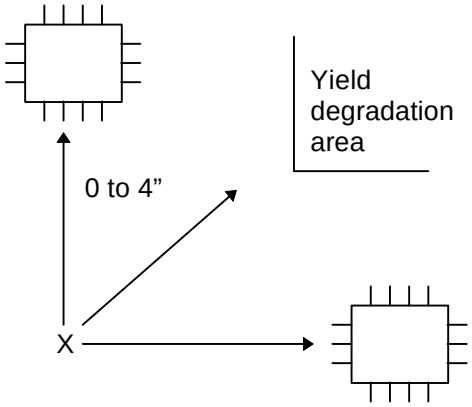


Figure 9: TQFP Placement on Printed Circuit Boards

Correctly oriented 45 degree defect expectations (see Figure 9).

Inches from Center	1	2	3	4	5	6	7	8	9	10	11
0° - 90° Orientation	0	0	0	10x	20x	50x	100x	250x	500x		
45° Orientation	0	0	0	0	0	0	0	0	10x	20x	100x

In summary, placement of any 16 mil pitch device is the second largest influence over the defect rate.

Raw Card and Stencil Image Attributes

The image reproduction accuracy of the raw PWB and stencil are critical in obtaining and sustaining a satisfactory defect rate with widely spaced 16 mil pitch devices. The stencil can only be aligned at one point on the PWB image. Any mis-registration approaching a full space between the 16 mil pitch leads (0.006”) will start causing shorts at tens of thousands of PPM.

Typical commercial PWB fabrication processes have not comprehended the need for very accurate and repeatable images on the active side of the PWBs. Research indicates that the specification and requirements for image registration are not well defined. The old hole true position registration plays very little part in the sub 20 mil pitch assembly process. Some points of reference were obtained. One supplier suggests an image registration accuracy of ± 0.002 inches (0.00011 inch per inch) over a 24 by 18 inch fabrication panel. This experiment substantiated that level of registration misalignment.

PWB Image Mis-Registration

Test Board dimensions	Mean X	3 Sigma X	Mean Y	3 Sigma Y	Inches per Inch
15 inches	0.0018	0.0024			0.00012
6 inches			0.00136	0.00138	0.00025

Conclusion Use of widely spaced 16 mil pitch devices will require an image registration tolerance specification and lot testing at the supplier to insure compliance. Anything over 0.00015 inch per inch will start to degrade the defect rate.

The stencil image registration is just as important as the PWB. It has been our experience that stencil images are as hard to control as the PWB image. Secondly, the image will move with print cycles. The movement is somewhat predictable.

Conclusion Just like the PCB every stencil image registration must be specified and verified when first purchased. Maximum mis-registration should be ± 0.002 over 13 inches (0.00015 inches per inch). If the dimensional registration of the board and stencil are at alignment extremes, it would be prudent to rebuild the stencil to better match the board registration trends. The maximum mismatch allowable including the stencil vision alignment accuracy is 0.005 inches before significant defects occur. Also, compensating a stencil to match board lots was felt to be counterproductive.

The Stencil Process

Following are the characteristics of the stencil equipment and process: (Equipment capability is critical to the defect rate.)

Stencil Printer	MPM UP 3030
Stencil Alignment Accuracy	± 0.0003 inches
Solder Paste Type	Alpha 609
Solder Paste Particle Size	325 to -500
Stencil Thickness	0.006 Laser Cut 301 Stainless Steel
Squeegee Type	Metal
Paste Actual Thickness	Mean = 0.0069 inches
Average 9 Boards, 3 Devices 10 Leads per Device	3 Sigma = 0.00073
Paste Volume	Mean = 3110 $mils^3$
3 Sigma Paste Volume	3 Sigma = 281 $mils^3$

Component Placement Process

Following are the characteristics of the placement process:

Placement Equipment	Fuji IPIII Placer
Placement Accuracy	± 0.0015 inches

The parts were placed on the pads using two local Fiducials per device.

Conclusion The placement was aligned with local Fiducials and the devices were placed in the center of the pads. Placement was not considered a significant contributor to the defect rate.

IR Reflow Characteristics

Following are the characteristics of the solder paste reflow process. Our standard reflow profile for this type of board was used.

IR Reflow Oven	Full convection BTU MN: TRS21
Atmosphere	Shop Air (no nitrogen)
Chain Speed	40 inches per minute
Max Temperature	215° C
Time Over 183° C	90 Seconds

Conclusion The IR reflow profile has the least effect on the 16 mil defect rate. A profile read out is shown on Figure 12.

Overall Conclusion Special attention to design and the assembly process is critical to assembly of widely spaced 16 mil pitch devices. Closely spaced 16 mil pitch devices offer lower defect rates. With proper design, the most important is placement and lead rotation, widely spaced 16 mil devices can be assembled with defect rates approaching 20 mil pitch devices. Not paying attention to a few basic requirements can make a product un-manufacturable and cost the manufacturer $20s of dollars per board in touch up costs. A truly non value added and avoidable expense.

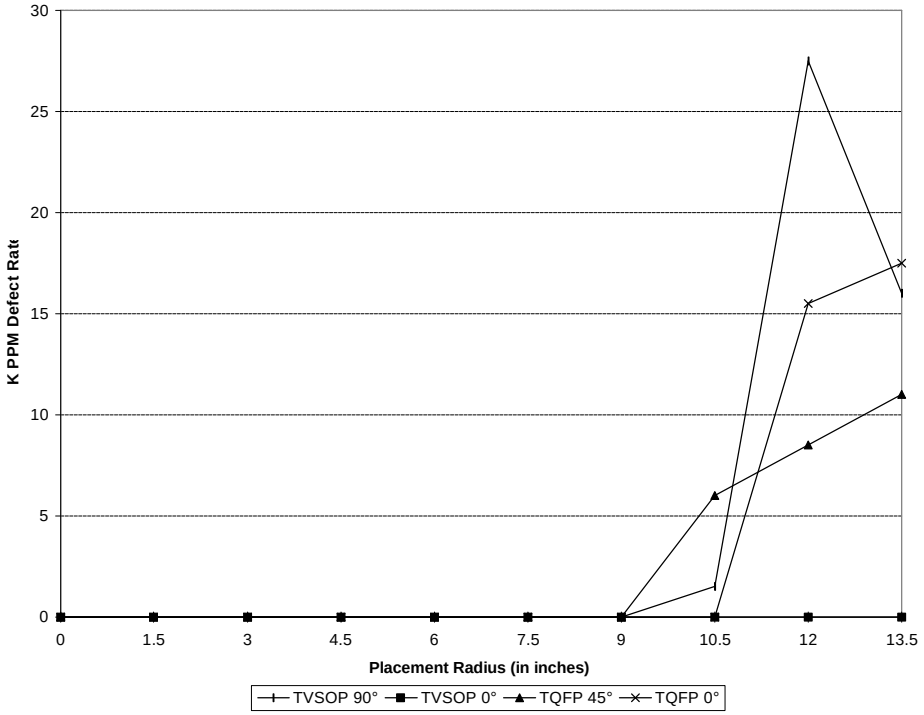


Figure 10: Defect Rate with 5 mil Stencil Thickness

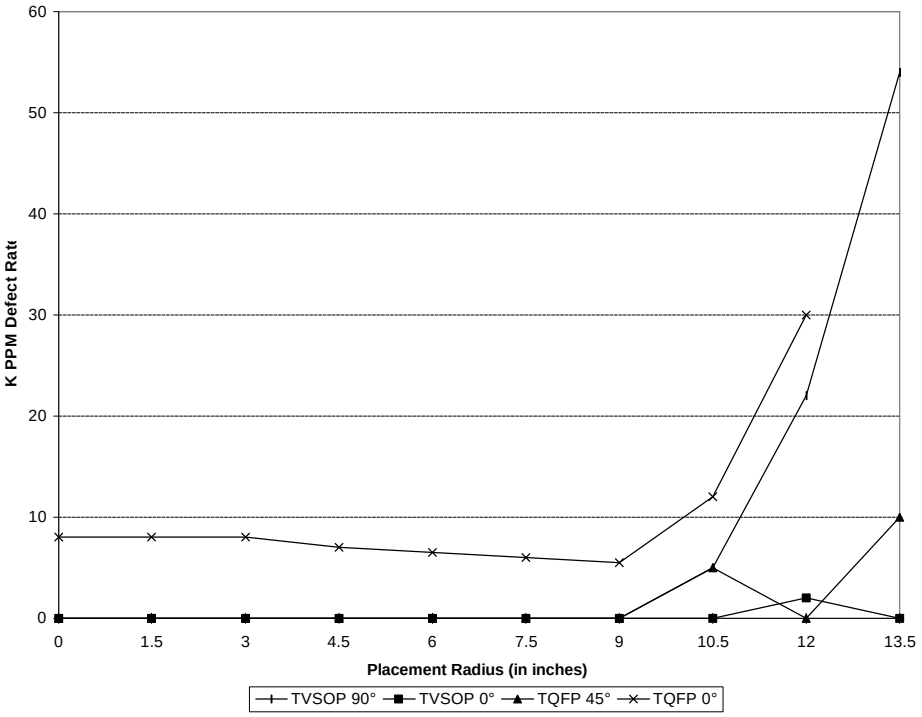
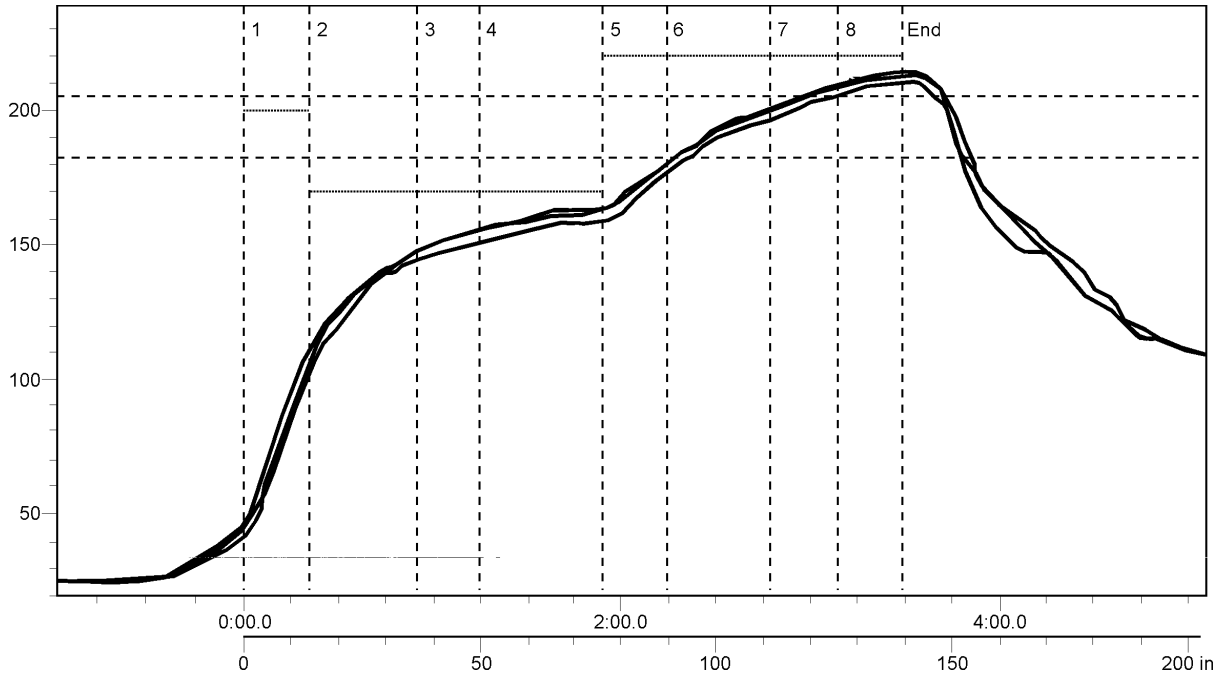


Figure 11: Defect Rate with 6 mil Stencil Thickness



	Zone	1	2	3	4	5	6	7	8
Speed	Upper	200°	170°	170°	170°	220°	220°	220°	220°
40 (in/min)	Lower	200°	170°	170°	170°	220°	220°	220°	220°

Figure 12: IR Reflow Thermal Profile

TVSOP Results from AVEX Electronics

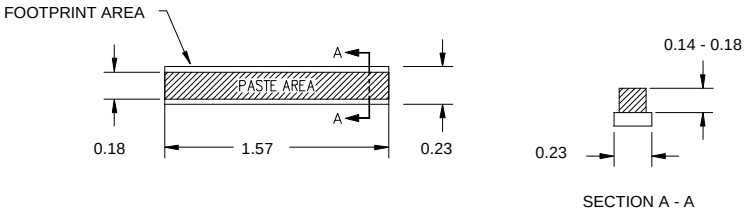
AVEX ELECTRONICS, INC.
Huntsville, AL
A Subsidiary of J.M. Huber Corporation

A total of 56 individual double-sided PCMCIA assemblies, located 8 to a manufacturing panel, for each of two types of plating, gold and Entek™, were manufactured by AVEX Electronics Inc.. Experiments were run on each of the assemblies to investigate the effect of pad geometry, stencil geometry and assembly process flow on 16 mil (0.4 mm) lead pitch components using high volume manufacturing equipment.

Pad and Stencil Geometry Requirements

The dimensions of the interconnect pad and stencil aperture have a major effect on the quality of the solder joint. These dimensions must be adhered to in the board design. The raw card and stencil must be produced to maintain these dimensions; otherwise yields and reliability will be significantly reduced.

The following dimensions were used for 16 mil pitch components using PCMCIA cards:



All Dimensions in mm

Figure 13: TVSOP Pad and Stencil Geometry for IR Reflow Solder Process

Pad Geometry:

Terminal Pad Length	0.062” (1.57 mm)
Terminal Pad Width	0.009” (0.23 mm)
Terminal Pad Pitch	0.016” (0.4 mm)
Pad Finish	Entek™, Gold Plating

Stencil Geometry:

Stencil Opening Length	0.062” (1.57 mm)
Stencil Opening Width	0.007” (0.18 mm)
Stencil Thickness	0.005” (0.13 mm)

Assembly Process

Figure 14 shows the assembly process flow conducted by AVEX Electronics for TVSOP packages.

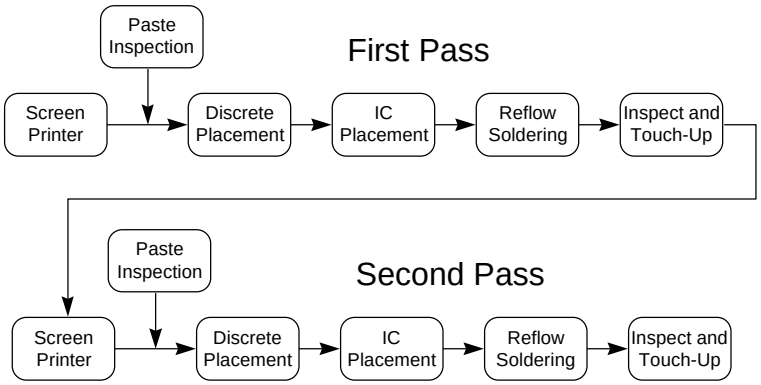


Figure 14: AVEX TVSOP Process Flow

The equipment used for the fine pitch mounting evaluation are listed below:

Screen Printer	DEK 265GS
Stencil Alignment Accuracy	± 0.0006 inches
Solder Paste	Alpha WS609
Solder Paste Particle Size	325 to 500 (25-45 microns)
Stencil Thickness	0.005 inches
Squeegee Type	Metal
Paste Actual Thickness	0.0055 to 0.007 inches
Paste Inspection	Cyberoptics LSI
Vision Placement	KME CM82 (for Discretes) KME CM92 (for IC's)
Vision Accuracy	± 0.001 inches
Reflow Oven	Heller 1700D

Process Reflow Profile

Following is the recommended IR reflow used. The IR Reflow profile below is standard for PCMCIA cards.

Preheat — Solder joint temperature must be gradually increased from ambient temperature to approximately 170° Celsius at a temperature ramp not to exceed 2.5 degrees per second

Soak — Solder joint temperature should be held at approximately 170° Celsius for a period of time not to exceed 50 seconds.

Reflow — Solder joint temperature must be increased from 170 to 210° Celsius at a temperature ramp rate not to exceed 2.5 degrees per second. Temperature dwell time above 183 degrees Celsius may range from 45 - 65 seconds. Total heating dwell time may be 4 - 6 minutes depending on thermal inertia and component sensitivity.

Conclusion

Based on the experiments during the TVSOP Qualification run, AVEX has drawn the following conclusions:

1. There was no appreciable difference between the gold and Entek™ plated PCB's. Choice of PWB plating materials should be based on the solder paste chemistry requirements.
2. Results comparing 7 and 8 mils aperture sizes showed that the smaller aperture resulted in a better yield.
3. Special consideration must be given to the screen print process, i.e., stencil thickness, aperture size and PWB support during the second pass screen print process.
4. Dedicated tooling may be required for machine placement on PWB's less than 0.031" thickness
5. Component inspection is critical and may require laser inspection capability on placement equipment.

Solder Joint Reliability Study

The following photo-micrographs are cross-sections of TVSOP leads attached to simulated PCMCIA circuit cards.

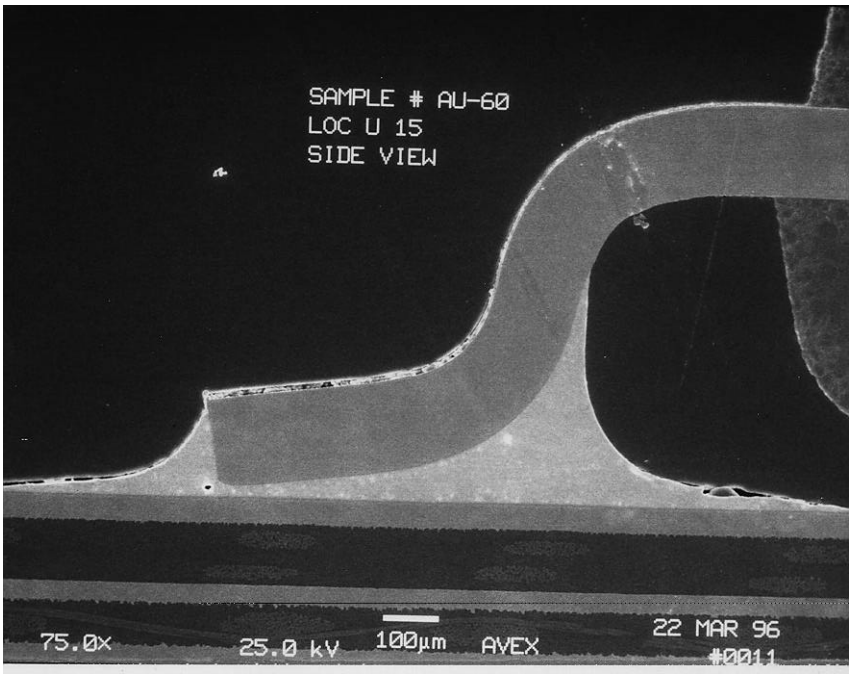


Figure 15: Cross Section (side view) of a TVSOP Lead to Pad Solder Joint

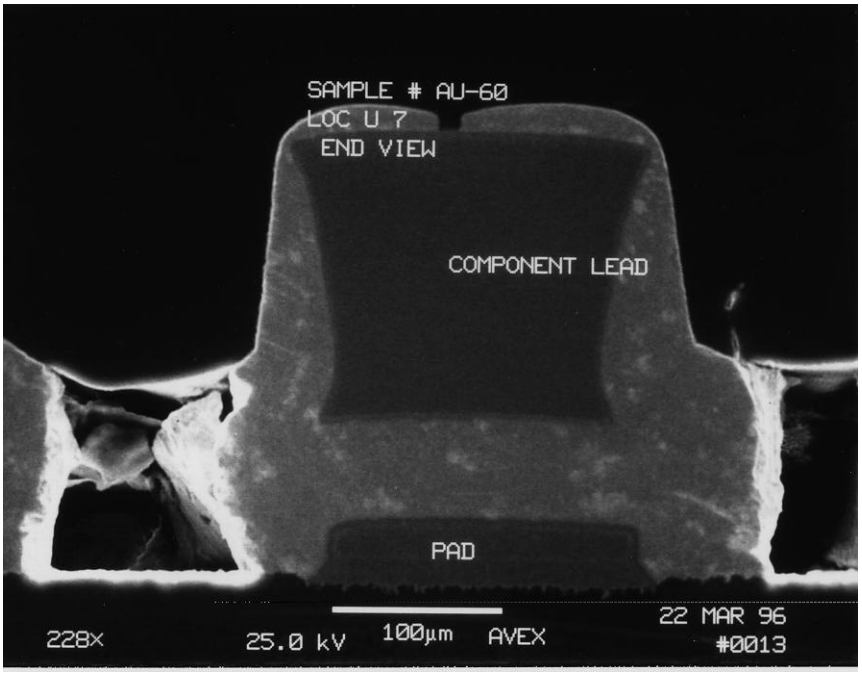


Figure 16: Cross Section (end view) of a TVSOP Lead to Pad Solder Joint

Temperature Cycle Test

This experiment was designed to determine the reliability of TVSOP solder joints.

No failures were obtained after 1200 thermal cycles between 0° - 100° Celsius. The following describes the AVEX thermal cycling test procedure and requirements for the TI PCMCIA Environmental Stress Screening (ESS).

- Support testing of 48 PCB's (12 panels) per run.
- 300 cycles (0 - 100° C Temperature Profile, 15 minute dwell time, 15 minute ramp).
- 900 cycles (0 - 100° C Temperature Profile, 7.5 minute dwell time, 7.5 minute ramp).
- No power source is required for Unit Under Test (UUT).
- UUT Continuity Test requiring monitoring of 2 circuits per UUT.
- No current load required on UUT traces.
- Continuous monitoring of UUT Status, sample rate of at least 1 sample/second.
- Failures to be removed after return to 25 degrees Celsius.

Test Implementation

The PCMCIA panel assemblies were loaded onto an AVEX standard ESS tray. The tray was modified to hold 5 panels per tray on metal screws with nylon standoffs. The standard ESS frame wiring was used to provide the I/O interface from the ESS chamber to a monitoring PC system. The PC system monitored the continuity of the UUT traces through a standard Digital I/O interface card.

Equipment List

The following equipment was used to perform the TI PCMCIA ESS test:

- ESS Chamber Model ESS5-7RWC
- AVEX ESS Frame
- 5 each AVEX tray assemblies
- Dell: 486/33 PC system
- Metrabyte: PIO96 Digital I/O card
- Application specific chamber to PC controller interface card assembly
- Application specific test software written in Borland C.

Chamber Profile

Temperature Range	0° C - 100° C	0° C - 100° C
Negative Ramp Time	15 Minutes	7.5 Minutes
Lower Dwell Time	15 Minutes	7.5 Minutes
Positive Ramp Time	15 Minutes	7.5 Minutes
Upper Dwell Time	15 Minutes	7.5 Minutes
Total Cycle Length	60 Minutes	30 Minutes
Number of Cycles	300 Cycles	900 Cycles
Total Continuous Cycles		1200 Cycles

Test Data

The ESS profile was run over the time period from 2/27/96 to 4/08/96. There were no test failures observed. The PC test data log contained no entries for state changes of the Digital I/O inputs.

Definitions and References

Definitions:

UUT - Unit Under Test. A single board assembly that is subjected to testing.

I/O - Input / Output. Signal lines for stimulus and monitoring of a system or board assembly.

PC System - IBM compatible personal computer system. Used as test controllers and monitoring units.

References:

AVEX Electronics: In-Line ESS Lab Setup Wiring Diagram, Document No. 4000-14-0159

AVEX Electronics: ESS Drawer block Diagram, Document No. 4978-08-2034

Texas Instruments Reference Information

Thermal Characteristics

Heat is transferred from packages in three ways; conduction, convection and radiation.

Conduction, the simplest heat-transfer mechanism, is the transfer of kinetic energy from a more excited electron to a nearby electron by method of vibrations and collisions. It is the primary mode of heat transfer within or between solids. Metals are good conductors as they possess high number of free electrons to encourage collisions. This ability to conduct heat is quantified by a proportionality constant (k) also known as thermal conductivity. The higher the thermal conductivity, the better the material is for heat conduction. Mold compounds play a role in conduction but do not contribute as much as copper leadframes.

The second method of heat transfer is convection. This transfer involves the movement of the heated substance. Convection is the primary mode of transfer between a solid, liquid or gas. The rate of convection is dependent on the surface area of the package and on the velocity and physical properties of air. Natural convection is heat transfer caused by induced differences in density that result from the expansion and contraction of air subjected to temperature changes. Forced convection is heat transfer caused by the movement of a cooling medium across a heat source. The presence of air flow increases the rate of heat transfer.

The third mode of heat transfer is radiation. Radiated heat transfers occur due to thermal emission primarily in the infrared spectrum. Though radiation always exists, it is the only mode of heat transfer between objects separated in a vacuum. Most of the heat transfer will take the form of conduction or convection.

Thermal Parameters

The thermal impedance (k-factor) of a package is defined as the increase in junction temperature above the ambient due to the power dissipated by the device and is measured in degrees Celsius per Watt. There are two indices commonly used to describe the thermal characteristics of an integrated circuit package, Θ_{JA} (junction to ambient) and Θ_{JC} (junction to case).

Junction Temperature is the temperature of the die inside the package. Maintaining the junction temperature within a given range is necessary for proper device functionality and for long term reliability. A lower junction temperature results in increased component reliability due to the reduced possibility of electro-migration or ball bond intermetallic failure. Table 4 illustrates this relationship.

Junction Temperature	Percent Failure Rate†
100° C	0.02
110° C	1
120° C	11
130° C	46
140° C	80
150° C	96

† Failure rate at 100,000 hours

Table 4: Junction Temperature vs. Long Term Reliability Comparison

Case Temperature is the temperature on the package surface measured at the center of the top of the package by an attached K-type thermocouple.

Ambient Temperature is the temperature of the surrounding air. It is usually used as a reference point to calculate the junction or case temperature. It is measured at some distance away from the device.

Thermal Measurements

In trying to make comparisons among parameters, it is important to understand how the parameters are measured and under what test conditions. Thermal measurement standards have been developed by JEDEC which will lead to a more consistent correlation of thermal performance between IC vendors. The JC15 JEDEC committee was formed to develop standards for the thermal measurement and modeling of IC packages. Perhaps the most important factor regarding variability in thermal measurements is the design of the thermal test board. Table 4 provides the JEDEC dimensions of dual-in-line packages with body length less than 28 mm and external lead pitch equal or less than 0.4 mm.

Dimension	Specification
Board Thickness	1.57 mm (0.062”)
Board Dimension (package length < 28 mm)	76.2 X 114.3 mm (3.0” x 4.5”)
Board Material	FR-4 Epoxy Glass
Fan-out Trace Length (minimum)	25 mm (0.98”)
Fan-out Trace Position	centered in 76.2 x 76.2 mm
Trace Thickness	0.071 mm (0.0028”) ± 20%
Trace Width for 0.4 mm lead pitch	0.4 mm (0.016”)

Table 5: JEDEC Thermal Test Board

Thermal modeling at TI uses an internally developed software package, ThermCal. The software divides the package into a large number of small elements (meshing) then calculates temperature for each element based on temperatures of the surrounding elements.

TVSOP Power Dissipation and Thermal Resistance Characteristics

Device junction temperature is mainly determined by the IC power consumption, the surrounding temperature and the thermal resistance between the junction and the atmosphere. The relationship is expressed by the following equation:

$$T_J = T_A + (\Theta_{JA})P$$

where: T_J = Junction Temperature
T_A = Ambient Temperature
P = Power
Θ_{JA} = Thermal Resistance

Equation 1: Junction Temperature Relationship

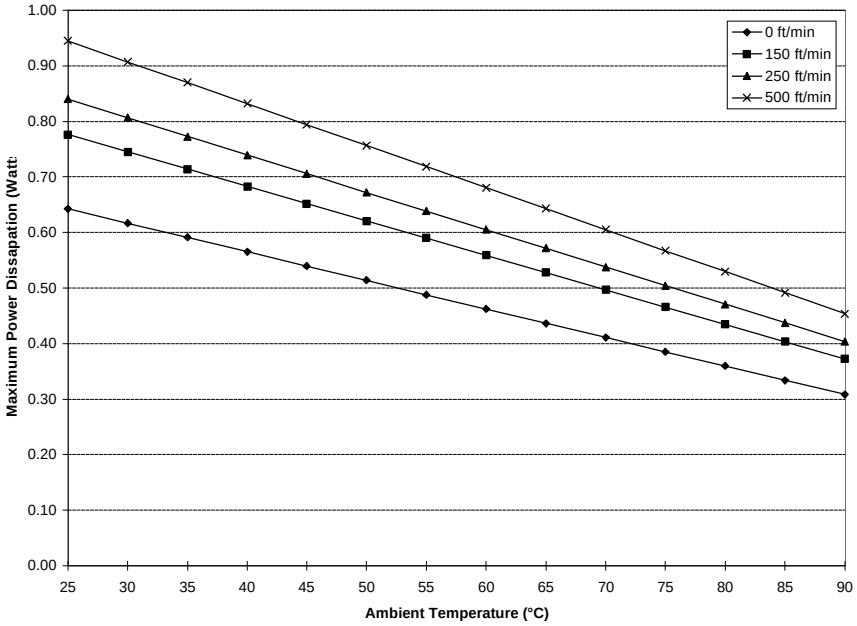
Thermal resistivity is the package's resistance to heat dissipation. Thermal resistivity is inversely related to thermal conductivity (k). When a device reaches a state of equilibrium, the electrical power delivered is equal to the thermal heat dissipated. This thermal energy is in the form of heat and is given off to the surroundings. The maximum allowable power consumption at a given surrounding temperature is computed using the maximum junction temperature for the chip:

$$P = \frac{(T_J - T_A)}{\Theta_{JA}}$$

Equation 2: Power Equilibrium Equation

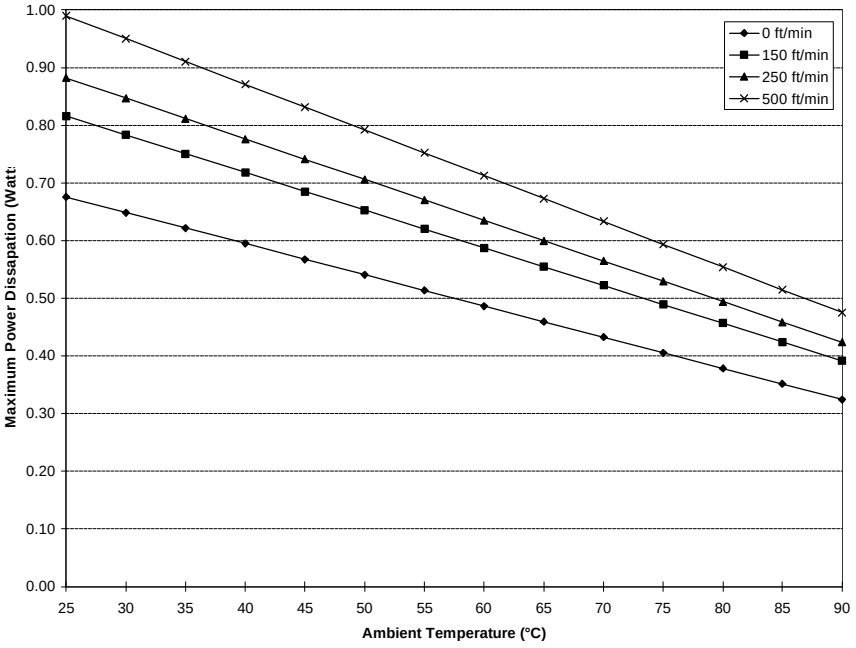
Figures 17 through 24 show the derating curves which were obtained from the above equation using the thermal resistance values determined by using Jedec standard boards with 1000 mil trace length and maximum junction temperature 150° C. The factors affecting the thermal resistance are mainly determined by material selection, geometry of packages, airflow, length and width of traces on board.

Natural convection, in many cases, is not enough for adequate heat dissipation. The solution is to induce airflow across a device. The data for TVSOP 48 package shows that migrating from natural convection to forced convection can decrease thermal resistivity by as much as 45 %.



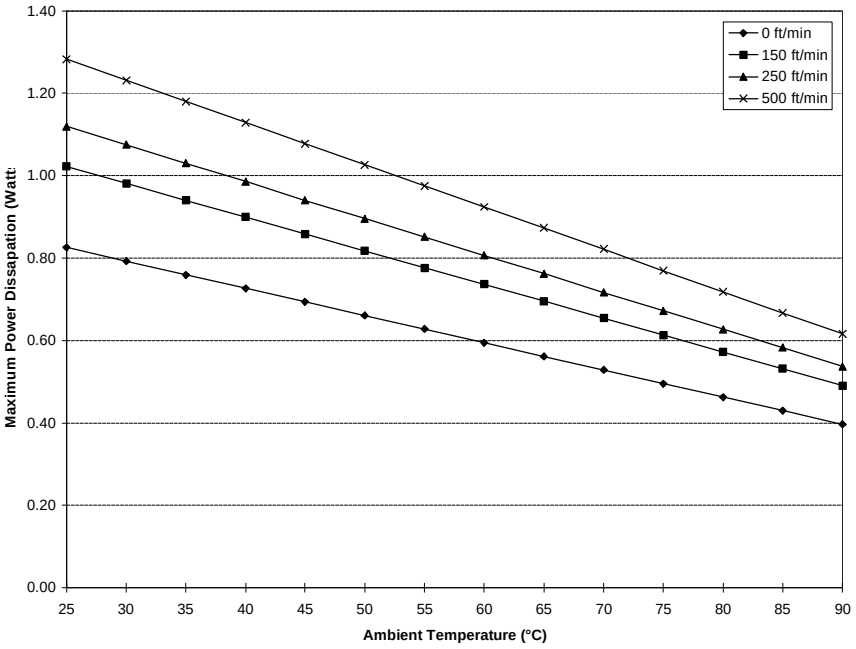
Air Velocity (ft/min)	0	150	250	500
Θ_{JA} (°C/W)	195	161	149	132

Figure 17: 14-pin TVSOP Derating Curves



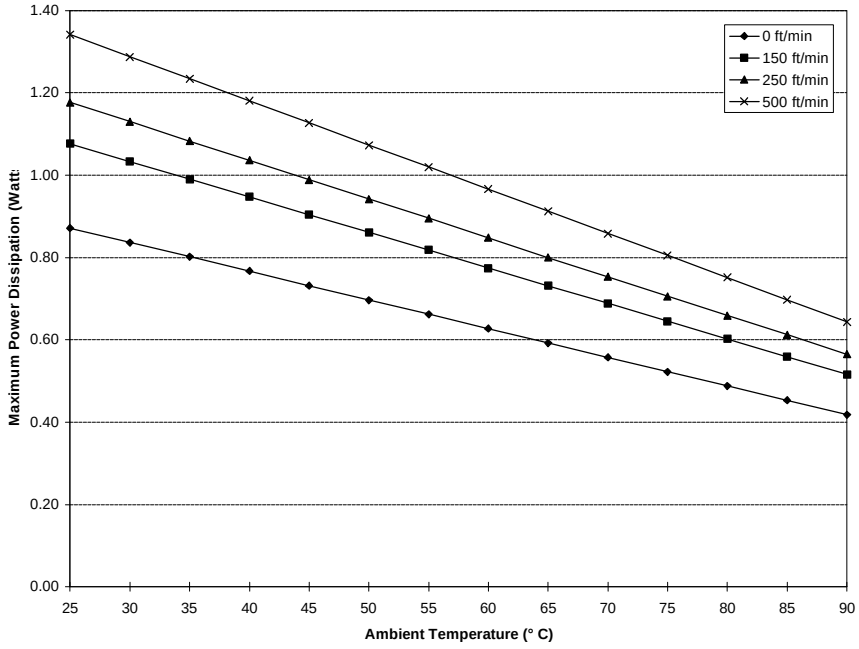
Air Velocity (ft/min)	0	150	250	500
Θ_{JA} (°C/W)	185	153	142	126

Figure 18: 16-pin TVSOP Derating Curves



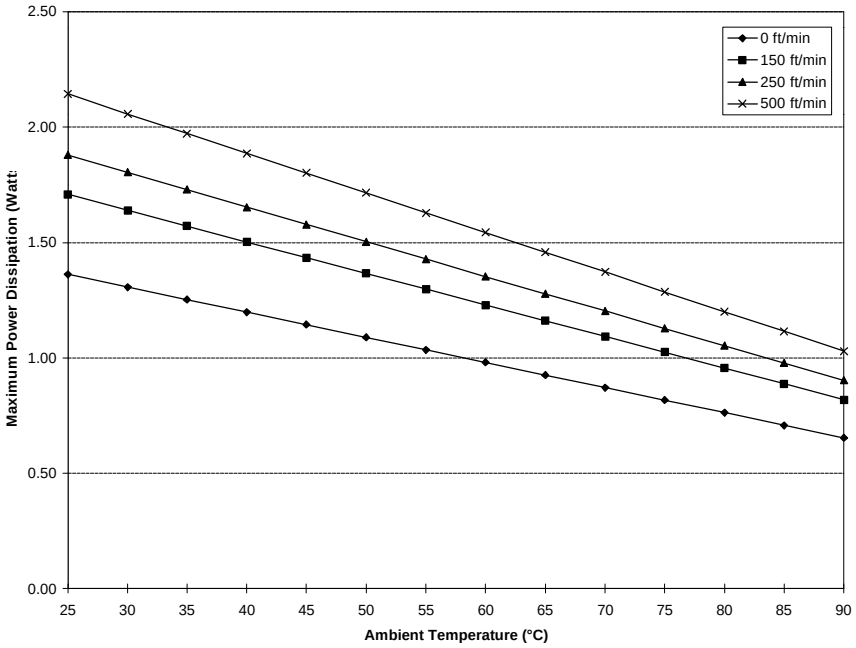
Air Velocity (ft/min)	0	150	250	500
Θ_{JA} (°C/W)	151	122	112	97

Figure 19: 20-pin TVSOP Derating Curves



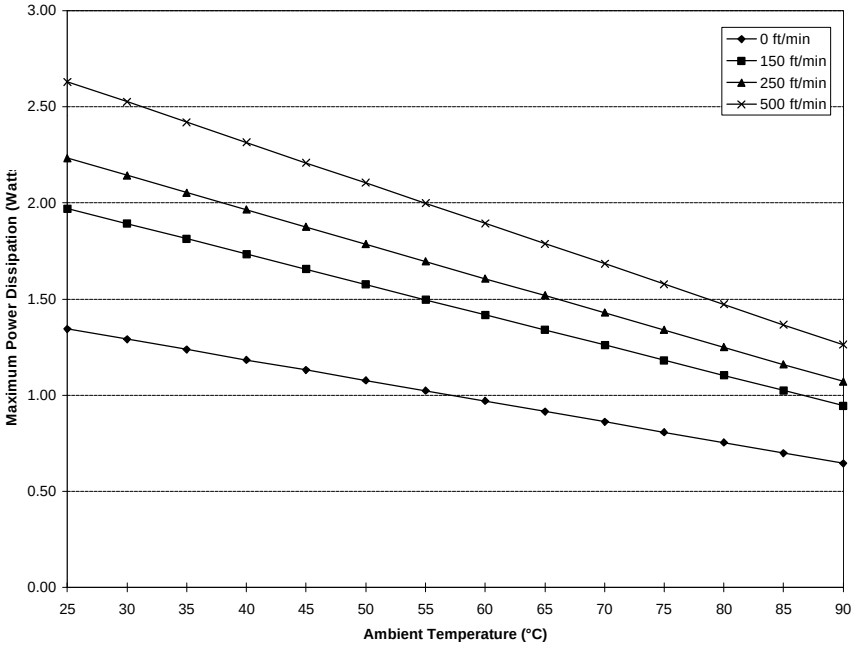
Air Velocity (ft/min)	0	150	250	500
Θ_{JA} (°C/W)	144	116	106	93

Figure 20: 24-pin TVSOP Derating Curves



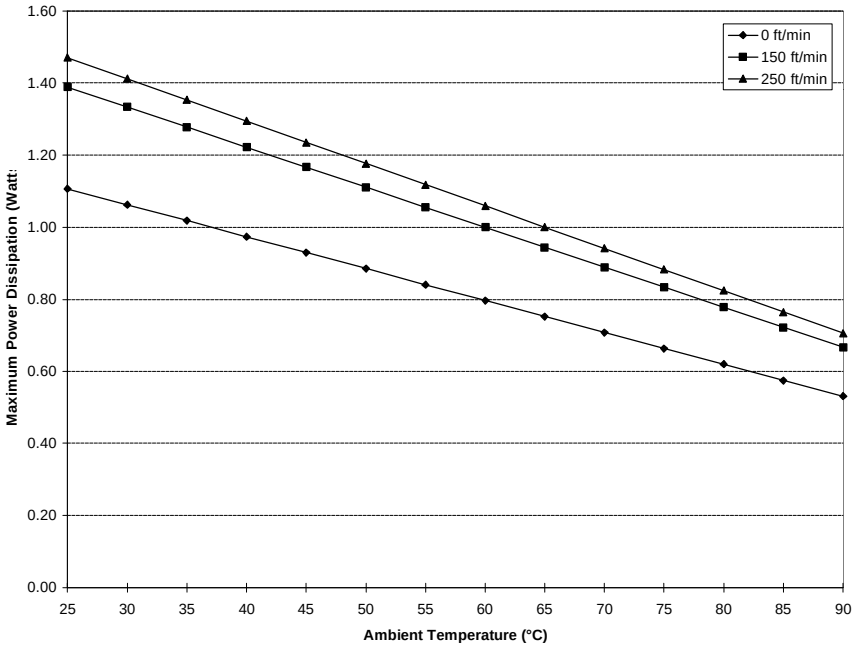
Air Velocity (ft/min)	0	150	250	500
Θ_{JA} (°C/W)	92	73	67	58

Figure 21: 48-pin TVSOP Derating Curves



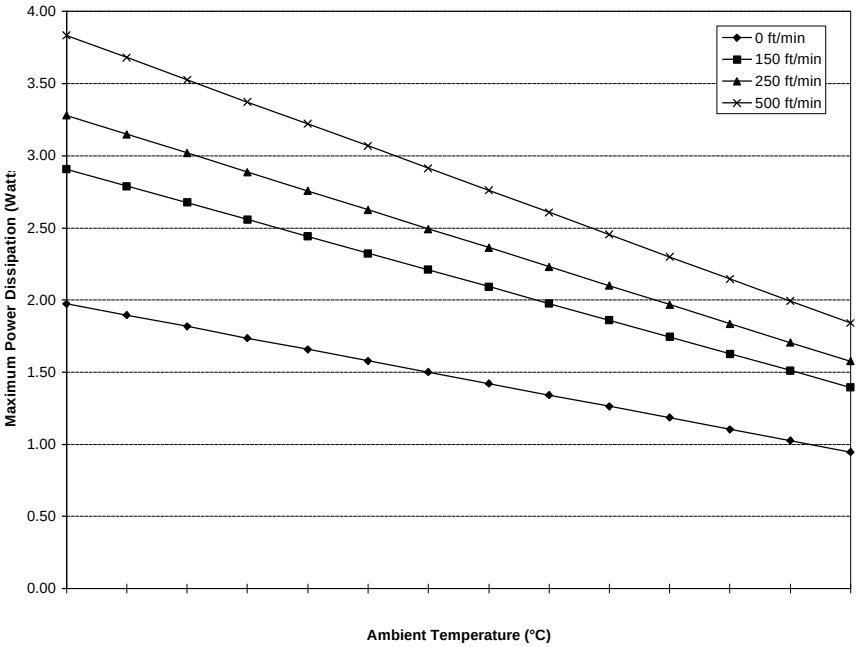
Air Velocity (ft/min)	0	150	250	500
Θ_{JA} (°C/W)	93	63	56	48

Figure 22: 56-pin TVSOP Derating Curves



Air Velocity (ft/min)	0	150	250
Θ_{JA} (°C/W)	113	90	85
Θ_{JC} (°C/W)	23.3		

Figure 23: 80-pin TVSOP Derating Curves



Air Velocity (ft/min)	0	150	250	500
Θ_{JA} (°C/W)	63	43	38	33

Figure 24: 100-pin TVSOP Derating Curves

Power Calculations[1]

When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (ICCL, ICCH, or ICCZ), while a CMOS device has a single value for ICC. These values can be found in the individual data sheets. TTL compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to VCC or GND; therefore, the input transistors are not switched completely off. This value, known as ΔICC, is also provided in the data sheet.

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd} which is listed in the data sheet and is obtained using the following equation:

$$C_{pd} = \left[\frac{I_{CC(dynamic)}}{(V_{CC}) f_i} \right] - C_L$$

Where: f_i = input frequency (Hz)
V_{CC} = supply voltage (V)
C_L = load capacitance (F)
I_{CC} = measured input current value (A)

Equation 3: Power Dissipation Capacitance

Although a Cpd value is not provided for ABT and other device types, the ICC versus frequency curves display essentially the same information. The slope of the curve provides a value in the form of a mA/(MHz • bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current.

Equations 2 through 6 can be used to calculate total power for CMOS, BiCMOS and bipolar devices:

$$P_{T(OTAL)} = P_{S(TATIC)} + P_{D(YNAMIC)}$$

Equation 4: Total Power

CMOS products with CMOS level inputs:

$$P_S = V_{CC}(I_{CC})$$
$$P_D = \left[(C_{PD} + C_L) V_{CC}{}^2 (f_1) \right] N_{SW}$$

Equation 5: Power Calculation for CMOS Input Levels

[1] The information presented in this section was copied in a slightly modified form from the Package Thermal Considerations Applications Note, SCZA002A. The information was also published in the Advanced BiCMOS Technology Data Book, SCBD002B, 1994, pp. 13-97 to 13-108 and other TI literature.

For TTL compatible CMOS products with TTL level inputs:

$$P_S = V_{CC}\left[I_{CC} + \left(N_{TTL}\right)\Delta I_{CC}\left(dc_d\right)\right]$$
$$P_D = \left[\left(C_{PD} + C_L\right){V_{CC}}^2\left(f_1\right)\right]N_{SW}$$

Equation 6: Power Calculations for TTL Input Levels

BiCMOS or Bipolar Products

$$P_S = V_{CC}\left\{dc_{en}\left[\frac{N_H\left(I_{CCH}\right)}{N_T} + \frac{N_L\left(I_{CCL}\right)}{N_T} + \left(1 - dc_{en}\right)I_{CCZ}\right] + N_{TTL}\left(\Delta I_{CC}\right)dc_d\right\}$$

Note: $\Delta I_{CC} = 0$ for bipolar devices

Equation 7: Static Power Calculation for BiCMOS or Bipolar Products

$$P_D = \left\{\left[dc_{en}\left(N_{SW}\right)V_{CC}\left(f_1\right)\left(V_{OH} - V_{OL}\right)C_L\right] + \left[dc_{en}\left(N_{SW}\right)V_{CC}\left(f_2\right)\left(\frac{mA}{MHz(bit)}10^{-3}\right)\right]\right\}$$

Equation 8: Dynamic Power Calculation for BiCMOS or Bipolar Products

Where:

V_{CC}	=	Supply Voltage (V)
I_{CC}	=	Power supply current (A), see data sheet
I_{CCL}	=	Power supply current (A) outputs low, see data sheet
I_{CCH}	=	Power supply current (A) outputs high, see data sheet
I_{CCZ}	=	Power supply current (A) outputs high impedance, see data sheet
DI_{CC}	=	Power supply current (A) CMOS inputs at a TTL level, see data sheet
dc_{en}	=	percent duty cycle enabled
dc_d	=	percent duty cycle disabled
N_H	=	Number of outputs in the high state
N_L	=	Number of outputs in the low state
N_{SW}	=	Number of outputs switching
N_T	=	Total number of outputs
f_1	=	Operating frequency (Hz)
f_2	=	Operating frequency (MHz)
V_{OH}	=	Output voltage (V) in the high state
V_{OL}	=	Output voltage (V) in the low state
C_L	=	External load capacitance (F)
$mA/(MHz \bullet bit)$	=	Slope of the I_{CC} vs. frequency curve

Electrical Characteristics

Mike Lamson, TI Process Automation Center
Maria Balian, ASL New Package Development

The electrical characteristics of the IC packages used at TI are normally determined by computer modeling programs developed in-house (PACED[2]) or commercially available software. Electrical parameters are also measured in our laboratories to verify the modeling data. The measurement methods follow the EIA/JEDEC Guideline EIA/JEP123 and include the use of Impedance Meters, Time Domain Reflectometers (TDR's) and Network Analyzers.

The electrical modeling program calculates the following parameters:

- Resistance (R) - DC or with high frequency effects
- Capacitance (C) - including loading and coupling capacitance
- Inductance (L) - including self and mutual inductance

The RLC parameters are available for each pin of the package being modeled or reported in tabular form as a range of values for the longest to the shortest leads. A SPICE input file for the package is also created by the modeling program. The SPICE file is produced in two formats: a lumped parameter file where each lead and bond wire is represented by one RLC element or a distributed parameter file where the lead and bond wire is represented by many RLC elements. The distributed version represents varying sections of the lead more accurately and is used for higher frequency simulations.

The characteristic impedance (Z_O) is also calculated for each section of the lead and bond wire. This may be important if impedance matching is a consideration in the design for high speed applications.

Electrical Parameters

Resistance

The resistance of an IC package conductor can be significant in certain package families as a source of IR voltage drop. In molded packages with copper (ρ=1.7 μohm-cm)[3] lead frames, most of the resistance is due to the bond wire because of the very small cross section (100 milliohms/0.1in.). If alloy 42 (ρ=48.8 μohm-cm) lead frames are used, the resistance of the lead can be several hundred milli-ohms and therefore much higher than the wire bonds. Co-fired ceramic packages tend to have higher conductor resistance since the material used is a Tungsten/Glass mixture (ρ=25 μohm-cm). Other families which may have significant trace resistance include the thin film processed interconnects as in some multi-chip modules due to the low thickness of the conductors.

[2] PACED: TI Process Automation Center Electrical Design software
[3] ρ (rho): Electrical Resistivity

Capacitance

Capacitance is a function of the lead surface proximity and the dielectric constant of the insulating material. These surfaces include the conductor leads, the power and ground planes if any and the presence of floating metal such as heat spreaders. The electrical models for molded lead frame packages assume a ground plane exists in the PC board on which it is mounted. The capacitance to ground is usually very small for these style packages and most of the loading capacitance is due to interlead coupling. This coupling capacitance can be a source of crosstalk noise from lead to lead.

The relative dielectric constant can vary widely among package families. Mold compound have relative dielectric constants of 4 to 5, alumina ceramic packages range from 9 to 10 and some lead-zinc-borate solder glass materials can be as high as 33.

Changing the proximity of one conductor to another can affect the coupling capacitance to a third conductor. This is exploited in some designs by moving the ground plane closer to the conductor leads to reduce the interlead coupling.

Inductance

Inductance is a function of the current distribution in the package and the relative permeability of the conductor material. Because of the dependence on current distribution, the effective inductance of a lead will depend on the ground return path in the system. Moving a ground plane closer to the conductor lead will decrease the magnetic field around the lead and reduce the self and mutual inductance to the other leads. The lead width also significantly influences self inductance. Minimum inductance is achieved when the lead width to height-of-lead-from-ground-plane ratio is maximized. Bond wires are a significant source of inductance because of their very narrow effective width.

The proximity of floating, non-ferrous, metal, as in heat spreaders, will also decrease the effective inductance due to eddy currents flowing in these structures. The eddy currents flow in the opposite direction from the lead currents so the total magnetic field is reduced.

As frequency increases, the self inductance of the package lead will decrease. This is caused by the reduction of the magnetic field internal to the lead by the skin effect (current density greater near the surface of the conductor and less in the center). For copper lead frames, this effect is very small and can usually be ignored. For magnetic lead frame materials with higher relative permeability such as alloy42, the frequency dependence is large. For modern devices, however, the fast rise times dictate a high frequency bandwidth for the package and the alloy42 self inductance will approach that of copper.

Solutions for reducing the effective inductance, especially for ground and power leads, includes increasing the number of lead paths for that function and multiple wire bonding to the same package pin. Doubling the conductors, however, does not reduce the inductance by half. The mutual inductance between the leads prevents this from happening and if the leads are tightly coupled, the inductance may only decrease by 20 percent or so. To maximize the reduction of the

effective inductance, the leads serving the same function, such as ground or power, should be as far apart as possible.

TVSOP Electrical Data

Following are the electrical characteristics of TVSOP packages. Figures 25 through 28 show the minimum and maximum range of capacitance (C) and inductance (L) for 14 to 56-pin narrow body TVSOP packages and 80 and 100-pin wide body TVSOP packages.

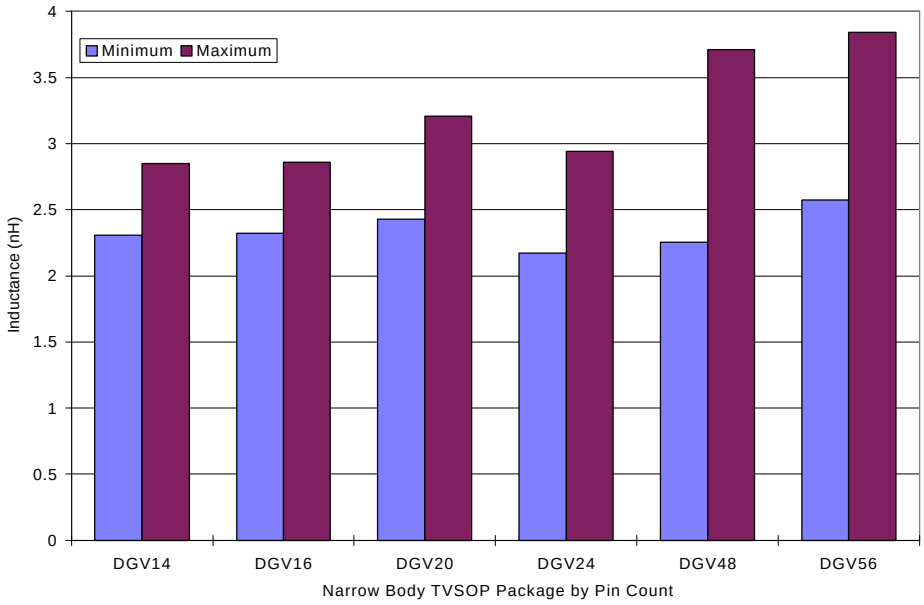


Figure 25: TVSOP Package Inductance (14, 16, 20, 24, 48 and 56-pin)

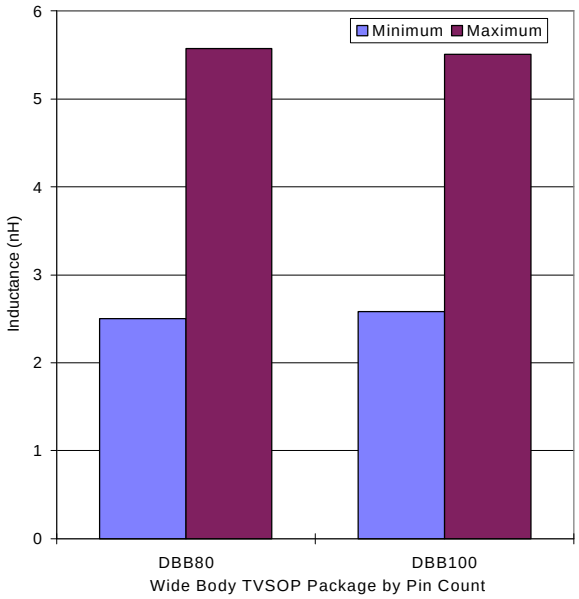


Figure 26: TVSOP Package Inductance (80 and 100-pin)

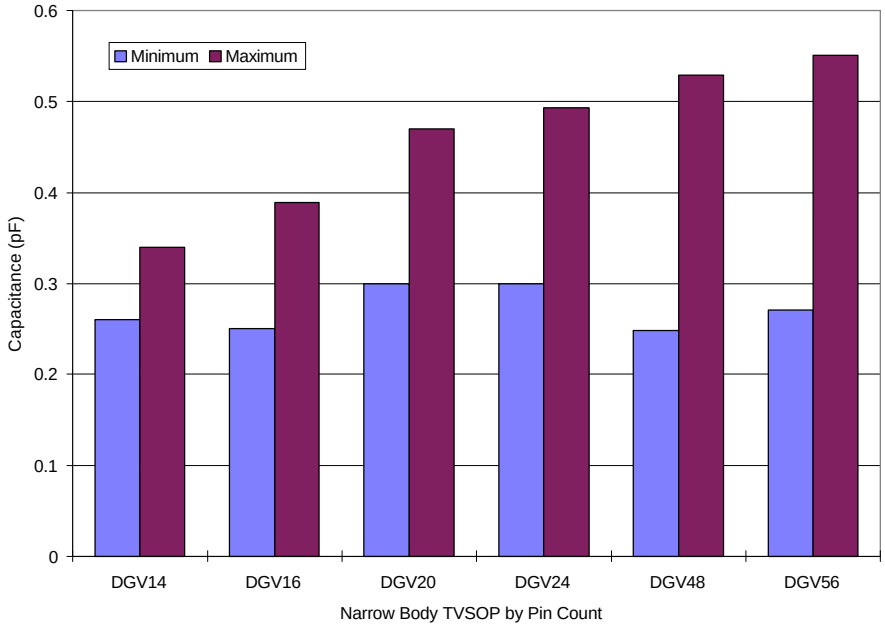


Figure 27: TVSOP Package Capacitance (14, 16, 20, 24, 48 and 56-pin)

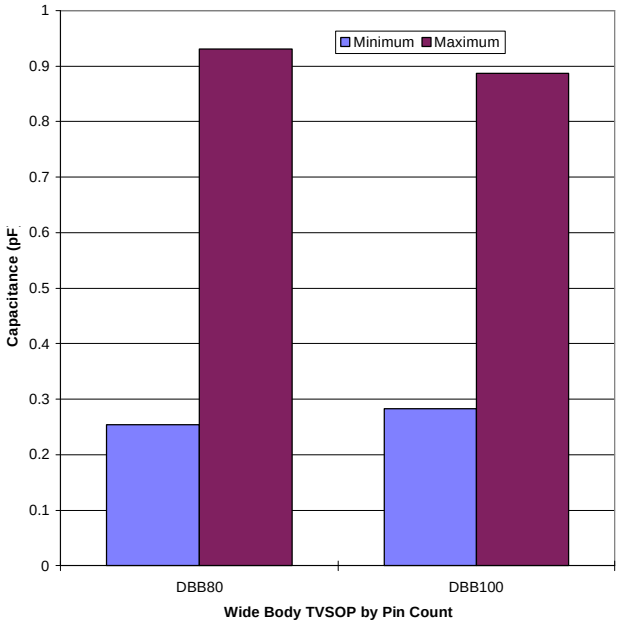


Figure 28: TVSOP Package Capacitance (80 and 100-pin)

TVSOP Package	Resistance (ohms)	Inductance L_S (nH)	Capacitance C_L (pF)
DGV 14	0.037 - 0.040	2.31 - 2.85	0.26 - 0.34
DGV 16	0.029 - 0.040	2.32 - 2.86	0.25 - 0.39
DGV 20	0.039 - 0.041	2.43 - 3.21	0.30 - 0.47
DGV 24	0.035 - 0.040	2.17 - 2.94	0.30 - 0.49
DGV 48	0.027 - 0.045	2.26 - 3.71	0.28 - 0.53
DGV 56	0.050 - 0.062	2.57 - 3.84	0.27 - 0.55
DBB 80	0.042 - 0.083	2.50 - 5.57	0.25 - 0.93
DBB 100	0.046 - 0.066	2.58 - 5.51	0.28 - 0.89

Notes:

1. Copper based leadframe and gold bond wire
2. Electrical values based on maximum die fit on packages
3. Ground plane is a single layer (no power or ground planes) and located on top of PCB board

Definitions:

L_S - Self inductance

C_L - Loading capacitance

Table 6: Summary of TVSOP Electrical Data

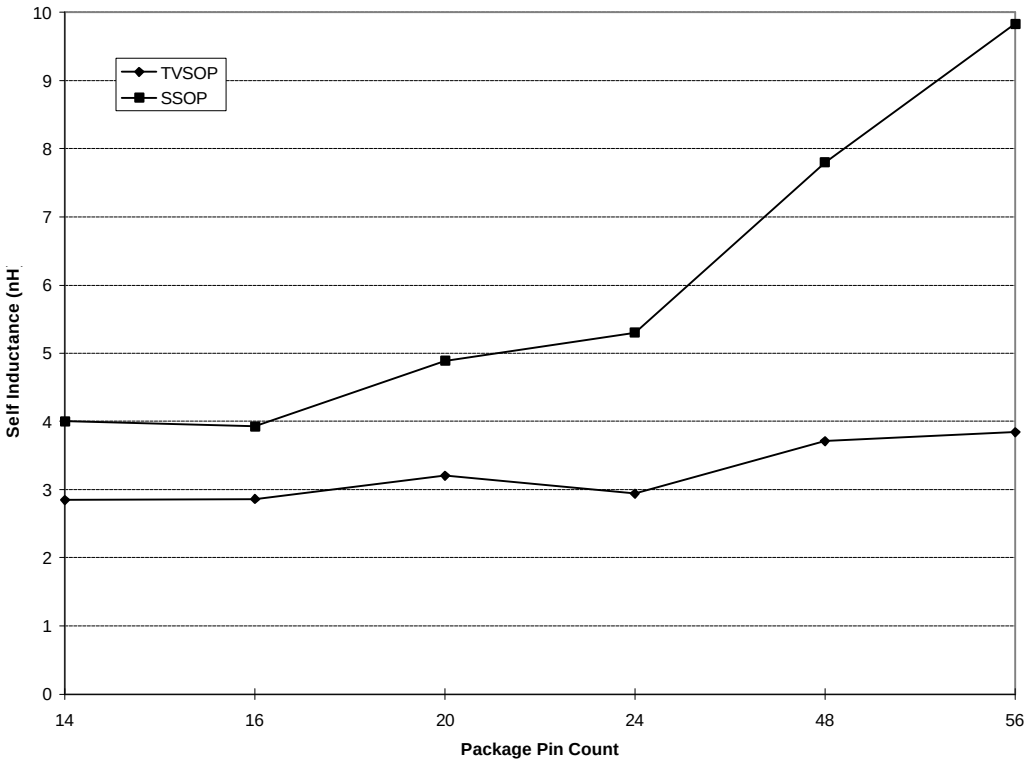


Figure 29: TVSOP and SSOP Self Inductance Comparison

Reliability Qualification Data

14-Pin TVSOP	Required SS / # Fails	AABT126DGV Act. SS / # Fails
Operating Life Static Test[1] 125° C, 1000 Hours	116/0	116/0
Biased Humidity[1] 85° C / 85% R H, 1000 Hours	116/0	116/0
Temperature Cycle Test[1] -65° C to 150° C, 1000 Cycles	116/0	116/0
Autoclave[1] 121° C, 15 psi, 240 Hours	76/0	76/0
Solderability	22/0	22/0
Solder Heat	22/0	22/0
Lead Fatigue	22/0	22/0
Lead Pull to Destruction	22/0	22/0
Lead Finish Adhesion	15/0	15/0
Flammability (UL)	5/0	5/0
Flammability (IEC)	5/0	5/0
Salt Atmosphere	22/0	22/0
X-ray - Top View Only	5/0	5/0
Manufacturability	Pass/Fail	Pass
Physical Dimensions	5/0	5/0
Moisture Sensitivity (Level 1)	12/0	12/0

Notes:
1. Condition level 1 preconditioning sequence:
   a) 85° C/85 % relative humidity for 168 hours with no bias, then
   b) Board mount (DGG, PH, PM. PN, PZ and RC packages only), then
   c) A 215° C IR solder reflow simulation, a 5 minute room temp delay, another IR solder reflow simulation, then
   d) Device clean-up with an isopropyl alcohol rinse, a de-ionized water rinse and one hour 25° C drying period.

Table 7: 14-pin TVSOP Package Reliability Results

20-Pin TVSOP	Required SS / # Fails	LVT244ADGV Act. SS / # Fails
Operating Life Static Test[1] 125° C, 1000 Hours	116/0	116/0
Biased Humidity[1] 85° C / 85% R H, 1000 Hours	116/0	116/0
Temperature Cycle Test[1] -65° C to 150° C, 1000 Cycles	116/0	116/0
Autoclave[1] 121° C, 15 psi, 240 Hours	76/0	76/0
Solderability	22/0	22/0
Solder Heat	22/0	22/0
Lead Fatigue	22/0	22/0
Lead Pull to Destruction	22/0	22/0
Lead Finish Adhesion	15/0	15/0
Flammability (UL)	5/0	5/0
Flammability (IEC)	5/0	5/0
Salt Atmosphere	22/0	22/0
X-ray - Top View Only	5/0	5/0
Manufacturability	Pass/Fail	Pass
Physical Dimensions	5/0	5/0
Moisture Sensitivity (Level 2)	20/0	20/0

Notes:
1. Condition level 2 preconditioning sequence:
   a) 85° C/60 % relative humidity for 168 hours with no bias, then
   b) Board mount (DGG, PH, PM. PN, PZ and RC packages only), then
   c) A 215° C IR solder reflow simulation, a 5 minute room temp delay, another IR solder reflow simulation, then
   d) Device clean-up with an isopropyl alcohol rinse, a de-ionized water rinse and one hour 25° C drying period.

Table 8: 20-pin TVSOP Package Reliability Results

48-Pin TVSOP	Required SS / # Fails	ABT16640DGV Act. SS / # Fails
Operating Life Static Test[1] 125° C, 1000 Hours	116/0	116/0
Biased Humidity[1] 85° C / 85% R H, 1000 Hours	116/0	116/0
Storage Life Test[1] 150° C, 1000 Hours	90/0	90/0
Temperature Cycle Test[1] -65° C to 150° C, 1000 Cycles	116/0	116/0
Autoclave[1] 121° C, 15 psi, 240 Hours	76/0	76/0
Solderability	44/0	44/0
Solder Heat	44/0	44/0
Lead Fatigue	6/0	6/0
Lead Pull to Destruction	6/0	6/0
Lead Finish Adhesion	6/0	6/0
Flammability (UL)	10/0	10/0
Flammability (IEC)	10/0	10/0
Salt Atmosphere	44/0	44/0
Resist Solvent	24/0	24/0
X-Ray - Top View Only	10/0	10/0
Manufacturability	Pass/Fail	Pass
Physical Dimensions	10/0	10/0
Moisture Sensitivity (Level 2)	20/0	20/0

Notes:
1. Condition level 2 preconditioning sequence:
   a) 85° C/60 % relative humidity for 168 hours with no bias, then
   b) Board mount (DGG, PH, PM. PN, PZ and RC packages only), then
   c) A 215° C IR solder reflow simulation, a 5 minute room temp delay, another IR solder reflow simulation, then
   d) Device clean-up with an isopropyl alcohol rinse, a de-ionized water rinse and one hour 25° C drying period.

Table 9: 48-pin TVSOP Package Reliability Results

80-Pin TVSOP	Required SS / # Fails	ALVC16901DBB Act. SS / # Fails
Operating Life Static Test[1] 125° C, 1000 Hours	120/0	120/0
Biased Humidity[2] 85° C / 85% R H, 1000 Hours	116/0	116/0
Storage Life Test[1] 150° C, 1000 Hours	45/0	45/0
Temperature Cycle Test[1] -65° C to 150° C, 1000 Cycles	120/0	120/0
Autoclave[1] 121° C, 15 psi, 240 Hours	78/0	78/0
Lead Fatigue	66/0	66/0
Lead Pull to Destruction	3/0	3/0
Lead Finish Adhesion	5/0	5/0
Salt Atmosphere	24/0	24/0
X-Ray - Top View Only	6/0	6/0
Manufacturability	Pass/Fail	Pass
Physical Dimensions	6/0	6/0
Moisture Sensitivity (Level 2)	12/0	12/0

Notes:
1. Condition level 1 preconditioning sequence:
   a) 85° C/85 % relative humidity for 168 hours with no bias, then
   b) Board mount (DGG, PH, PM. PN, PZ and RC packages only), then
   c) A 215° C IR solder reflow simulation, a 5 minute room temp delay, another IR solder reflow simulation, then
   d) Device clean-up with an isopropyl alcohol rinse, a de-ionized water rinse and one hour 25° C drying period.
2. Condition level 2 preconditioning sequence:
   a) 85° C/60 % relative humidity for 168 hours with no bias, then
   b) Board mount (DGG, PH, PM. PN, PZ and RC packages only), then
   c) A 215° C IR solder reflow simulation, a 5 minute room temp delay, another IR solder reflow simulation, then
   d) Device clean-up with an isopropyl alcohol rinse, a de-ionized water rinse and one hour 25° C drying period.

Table 10: 80-pin TVSOP Package Reliability Results

Delivery of the TVSOP to TI Customers

Moisture Sensitivity of the TVSOP

Moisture sensitivity describes the characteristic of some plastic surface mount packages to absorb sufficient moisture from their environment to cause package cracking when exposed to the extreme temperature of reflow soldering. During the reflow soldering (IR, VPR, or wave solder), flash vaporization of the absorbed moisture causes high stress resulting in internal cracking or delamination between the chip and the leadframe chip pad. Packages are tested for moisture sensitivity in accordance with JESD A112. Those packages which fail to meet Level 1 are designated as "moisture sensitive" and are dry packed. Table 9 describes the recommended floor life of the package after it is removed from the sealed dry pack bag prior to soldering. The floor life may be extended by sealing the dry pack bags as soon as possible after removing the components to be used.

	Floor Life	
Level	**Conditions**	**Duration**
1	≤ 30° C / 90% RH	Unlimited
2	≤ 30° C / 60% RH	1 Year
3	≤ 30° C / 60% RH	168 Hours
4	≤ 30° C / 60% RH	72 Hours
5	≤ 30° C / 60% RH	24 Hours
6	≤ 30° C / 60% RH	6 Hours

Table 11: TVSOP Moisture Sensitivity

Dry Pack is a method for protecting moisture sensitive plastic surface mount devices from moisture during shipment and storage. The parts are initially baked and then placed inside a moisture vapor barrier bag with a desiccant. The desiccant absorbs moisture and keeps the humidity inside the bag at a safe level. The moisture vapor barrier bag used in dry pack has a maximum transmission rate of 0.02g/100 square inches in 24 hours. The desiccant used can absorb up to 3 grams of water per unit at 20% Relative Humidity (RH). The actual shelf life will vary based on the storage conditions, the quality moisture barrier the bag provides, the number of desiccants used and the size of the package. A humidity indicator card is also added to the bag which shows the internal humidity of the bag in 10% increments. One can use this card to verify that the humidity level inside the bag has not exceeded the safe level. If the humidity inside the dry pack bag exceeds the recommended RH limit shown on the drypack label, the parts must be baked dry before soldering.

Baking conditions and duration are described on the drypack labels along with an outline of necessary precautions and seal date for products. TI uses this dry pack method regardless of whether the parts are shipped in tubes or tape and reel.

Moisture Sensitivity Qualification Data

Pin Count	Moisture Level
14-Pin	Level 1
16-Pin	Level 1
20-Pin	Level 2
24-Pin	Level 2
48-Pin	Level 2
56-Pin	Level 2
80-Pin	Level 2
100-Pin	Level 2

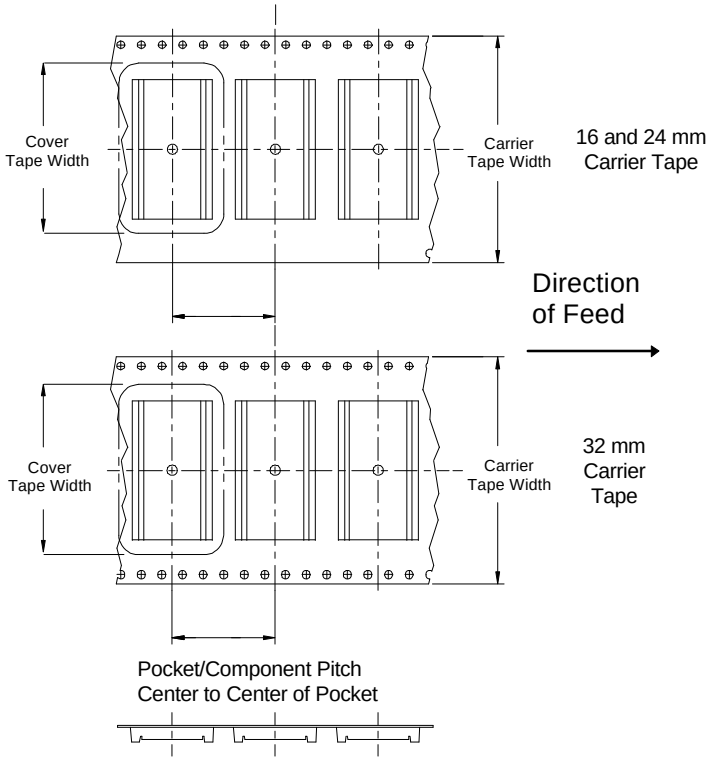
Table 12: TVSOP Moisture Sensitivity Levels

Further reliability tests have been submitted on 20 and 24-pin packages to determine whether they can be reclassified as “non-moisture sensitive” (level 1 moisture sensitivity).

Tape and Reel

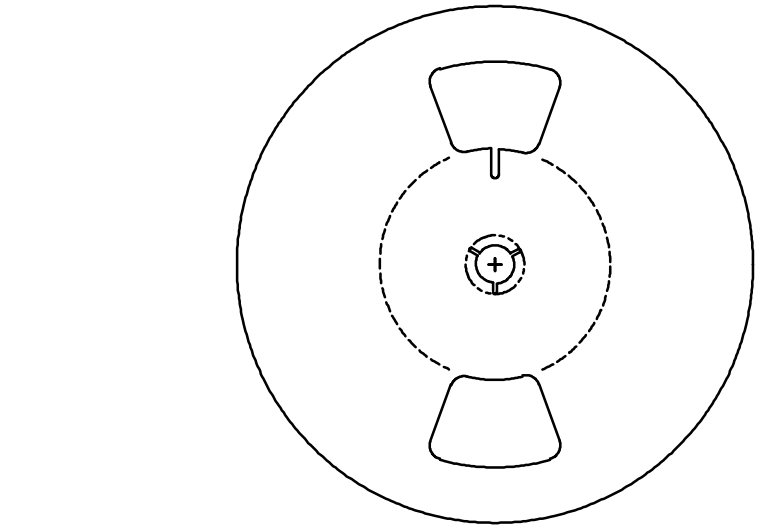
The purpose of this method of packaging is to position components such that they may be automatically placed. Components such as but not limited to diodes, capacitors, resistors, transistors, inductors and integrated circuits may be packed in this manner.

The packing materials used normally include a carrier tape, cover tape and a reel. All material used meets Industry guidelines for ESD protection. Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1, EIA-481-2 and EIA-481-3. The dimensions that are of particular interest to the end-user are tape width, pocket pitch and quantity per reel. The following figures illustrate typical designs for carrier tape and reels for TVSOP packages.



Package	Pins	Carrier Tape Width (mm)	Cover Tape Width (mm)	Pocket Pitch (mm)	Quantity per Reel
DGV	14-48	16.00	13.3	8.00	2000
DGV	56	24.00	21.0	8.00	2000
DBB	80	24.00	21.0	12.00	500
DBB	100	32.00	25.5	16.00	500

Figure 30: Carrier and Cover Tape Information for Reeled TVSOP Packages



Package Type (number of pins)	Carrier Tape Width	Cover Tape Width	Reel Width	Reel Diameter
DGV (14-48)	16.00	13.3	16.4	330
DGV (56), DBB (80)	24.00	21.0	24.4	330
DBB (100)	32.00	25.5	32.4	330

Dimensions in mm

Figure 31: Reel Dimensions

Test Sockets

The following table lists available test sockets from Yamaichi and Enplas (note that the sockets are 'closed tooling'):

Vendor	Pin Count	Socket with Flange	Socket without Flange
Yamaichi	14	IC51-0142-2074-MF	IC51-0142-2074
Yamaichi	16	IC51-0162-2073-MF	IC51-0162-2073
Yamaichi	20	IC51-0202-2072-MF	IC51-0202-2072
Yamaichi	24	IC51-0242-2071-MF	IC51-0242-2071
Yamaichi	48	IC51-0482-2069-MF	IC51-0482-2069
Yamaichi	56	IC51-0562-2067-MF	IC51-0562-2067
Yamaichi	80	IC51-0802-2077-MF	IC51-0802-2077
Enplas	80		FP-80-0.4-01
Yamaichi	100	IC51-1002-2076-MF	IC51-1002-2076

Table 13: Available TVSOP Test Sockets