Mixing It Up With 3.3 Volts

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Introduction

The evolution to a 3.3-V supply voltage is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M-bit versions will be developed for operation from a supply voltage of 3.3 ± 0.3 V. For 16M-bit DRAM products there is no such rule of thumb as certain vendors expect to operate from 3.3 V, while others will offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most 16M versions will operate at 3.3 V or lower (down to 2.7 V).

Typical 1M-bit DRAM geometries are on the order of 1.2 μm, and it is not a problem to apply a 5-V power supply to this type of product. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection which over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts. Therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V reduces the power consumed by the device which increases system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor towards 3.3-V operation.

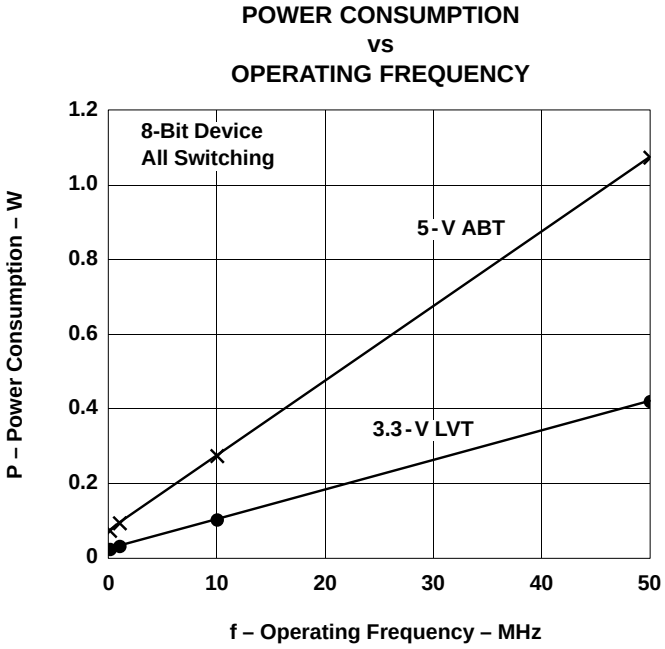

Figure 1. 3-V to 5-V Power vs Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards favor high performance over low power, but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebooks and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power such as laptop computers, automotive and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower buildup of heat due to lower power consumption, and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low-voltage products is one of increased battery lifetime.

Of all the end-equipment groups which can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as point-of-sale terminals which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on-board transmitter. The goal for these systems is to have a battery life of 8 to 10 hours, roughly the equivalent of one work day or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied, however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged but the spread actually runs from about 3.3 V up to 3.9 V. For now the unregulated battery market demands low-voltage products which are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 V, where devices will slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V, with volume requirements not beginning until the ’94–’95 time frame. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D converters, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies with supply voltages less than 3.3 V has been an issue since 1984 when two JEDEC standards were adopted. Standard 8.0 was intended to address both regulated (3-V to 3.6-V) and unregulated (2-V to 3.6-V) battery applications. Standard 8.1 was intended to address higher-performance applications operating from a regulated power supply that could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the most critical one being reviewed now. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems and contain a provision for battery-operated systems. Until this happens, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to V_{CC}. This limits input voltages to V_{CC} + 0.5 V and limits direct connection to a 5-V system.

Mixed-Mode Operation

This dilemma of device incompatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a serious industry concern. Mixed-mode operation allows for direct communication between the two systems. Devices which support this mode must be designed for maximum input voltages of 5.5 V without any long-term reliability issues. Another concern is that the output drive must be capable of driving a standard-TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS systems.

Figure 2 compares the standard-TTL dc interface levels with two of the emerging low-voltage standards. Low-voltage CMOS (LVCMOS) is a pure CMOS specification that specifies low current rail-to-rail output drive along with input voltage levels, V_{IH} and V_{IL}, which are ratios of V_{CC}. Low-voltage TTL (LVTTL) utilizes the standard-TTL input levels of 0.8 and 2 V as well as specifying a higher dc output drive than LVCMOS. To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet all of the requirements of the three different specifications.

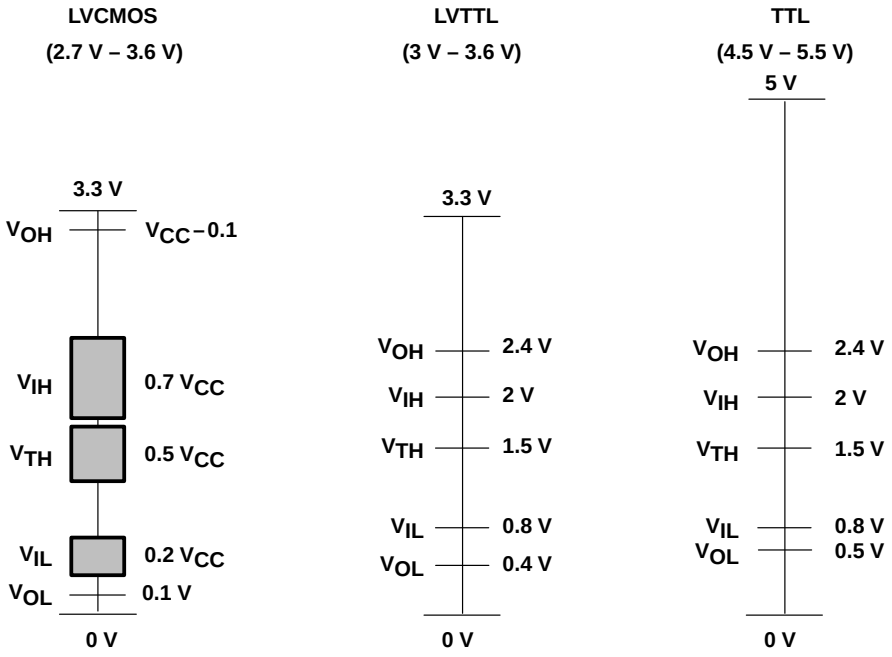

Figure 2. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices, and provides the following family characteristics:

5.5-V maximum input voltage

Specified 2.7- to 3.6-V supply voltage

I/O structures that support power-on (live) insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = –32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
$I_{CC(L)}$ = 15 mA
$I_{CC(H)}$ = 250 µA
$I_{CC(Z)}$ = 250 µA

Propagation delays of:
t_{pd} < 4.6 ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:
48- and 56-pin SSOP for LVT Widebus™
20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices, as shown in Figure 4, providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down applications or when live insertion is required.

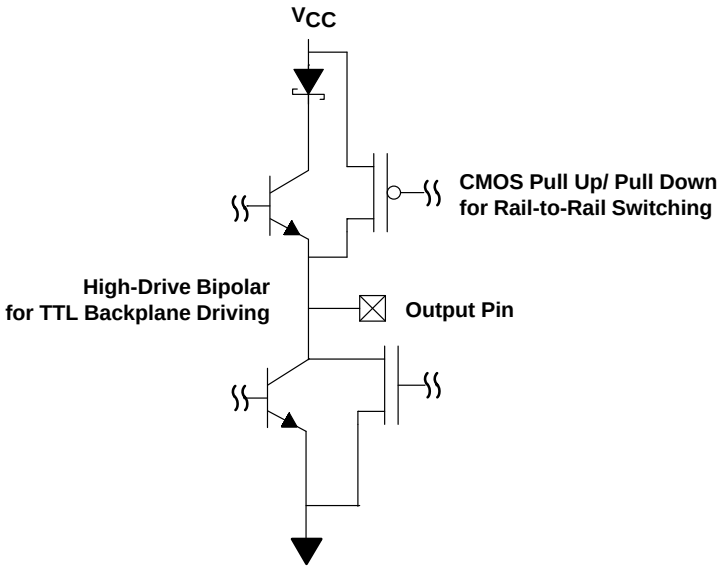

Figure 3. Simplified LVT Output Structure

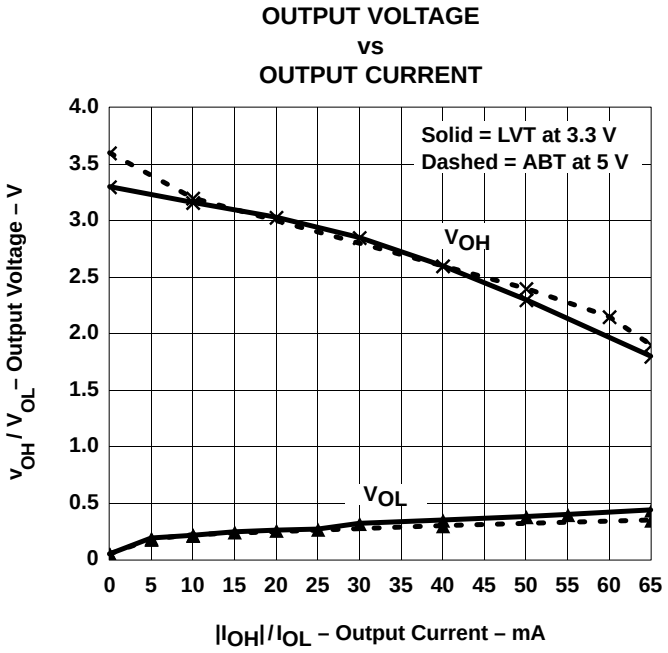

Figure 4. ABT vs LVT Output Drive Comparison

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ± 100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ± 500 μA, to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load, and does not affect the propagation delay of the driving output.

Summary

LVT devices solve the system need for a transparent interface between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live insertion or partial-power applications while providing low-input leakage currents. The outputs are capable of driving today's 5-V backplanes with a considerable reduction in the device's power consumption and are packaged in state-of-the-art fine-pitch surface-mount packages.