Implications of Slow or Floating CMOS Inputs

TEXAS INSTRUMENTS

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Introduction

In recent years, CMOS (AC, ACT, LVC) and BiCMOS (ABT, LVT) logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. The reason is very obvious: power consumption is becoming a major issue in today's market. However, when designing systems using CMOS and BiCMOS devices, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer requires as well as designing within the data sheet specifications. Because data sheets do not cover the input behavior of a device in detail, this application note explains the input characteristics of CMOS and BiCMOS families in general. It also explains ways to deal with problem issues when designing with such families where floating inputs are a concern. Understanding the behavior of these inputs results in more robust designs and better reliability.

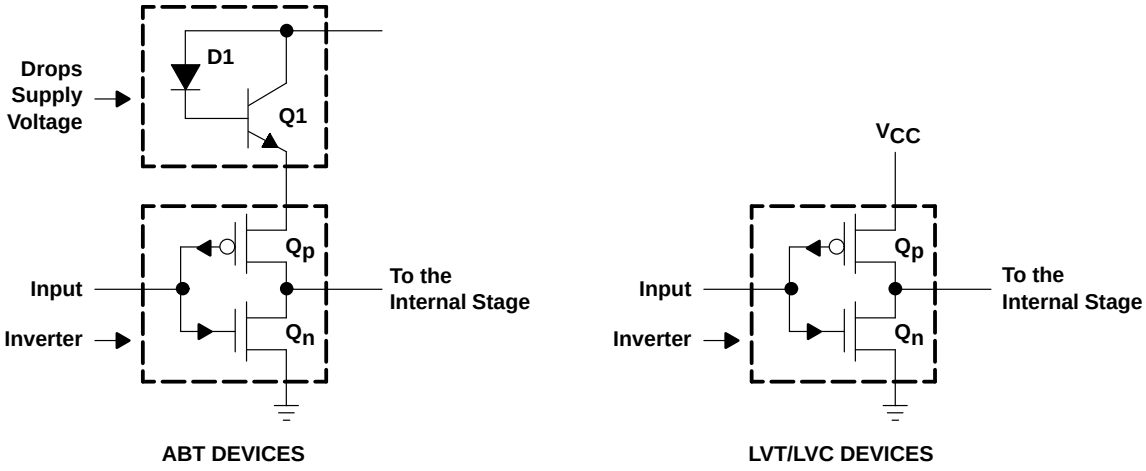

Figure 1. Input Structures of ABT and LVT/LVC Devices

Characteristics of Slow or Floating CMOS Inputs

Both advanced CMOS and BiCMOS (ABT/LVT) families have a CMOS input structure. This structure is an inverter consisting of a p channel to V_{CC} and a n channel to GND as shown in Figure 1. With low-level input, the p-channel transistor is on and the n channel is off, causing current to flow from V_{CC} and pulling the node to a high state. With high-level input, the n-channel transistor is on and the p channel is off and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region causing the n channel and the p channel to be turned on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 to 2 V). The supply current (I_{CC}) can rise to several milliamperes per input, peaking at approximately 1.5 V V_I (see Figure 2). This is not a problem when switching states at the data-sheet-specified input transition time (see Figure 3).

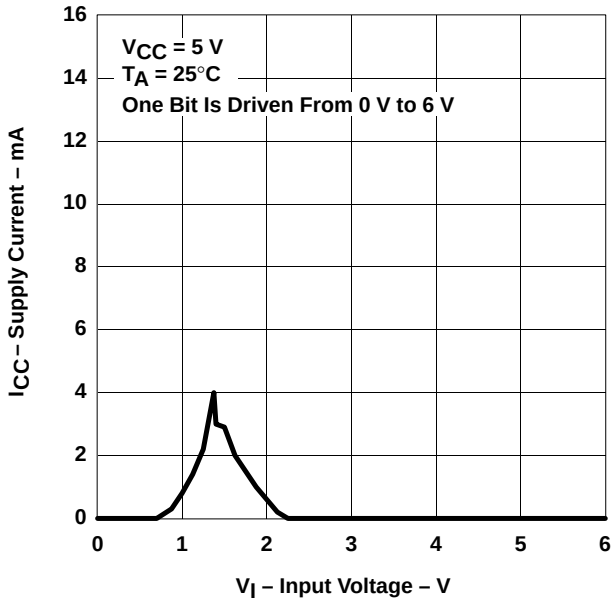

Figure 2. Supply Current Versus Input Voltage (One Input)

recommended operating conditions

			MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise or fall rate	ABT octals		5	ns/V
		ABT Widebus™ and Widebus+™		10	
		LVT, LVC, ALVC		10	
		LV		100	

Figure 3. Input Transition Rise or Fall Rate as Specified in Data Sheets

Slow Input Edge Rate

With increased speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations. Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.

These functional problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 4). Because the device's internal power supply nodes are used as voltage references throughout the integrated circuit, inductive voltage spikes, V_{GND}, affect the way signals appear to the internal gate structures. For example, as the voltage at the device's ground node rises, the input signal, V_I', appears to decrease in magnitude. This undesirable phenomena can then erroneously change the output if a threshold violation occurs.

In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_I', at the device will appear to be driven back through the threshold and the output will start to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge will be repeatedly driven back through the threshold, causing output oscillation. Therefore, the maximum input transition time of the device should not be violated so no damage to the circuit or the package can occur (refer to Figure 3 for the maximum transition rate for each family).

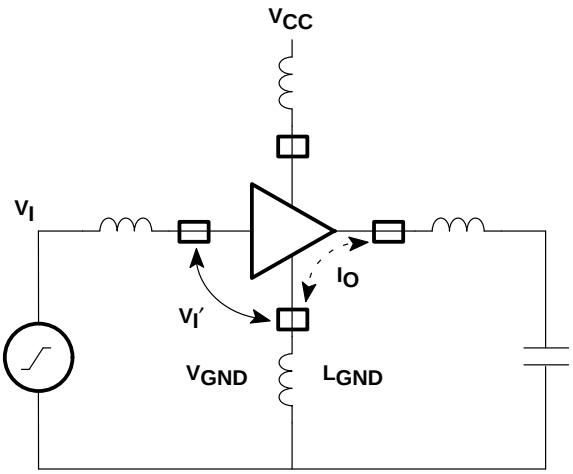

Figure 4. Input/Output Model

Floating Inputs

If a voltage between 0.8 V and 2 V is applied to the input for a prolonged period of time, this situation becomes critical and should not be ignored, especially with higher bit count and more dense packages (SSOP, TSSOP). For example, if an 18-bit transceiver had 36 I/O pins floating at the threshold, the current from V_{CC} could be as high as 150 to 200 mA. This is approximately 1 W of power consumed by the device, which leads to a serious overheating problem. This continuous overheating of the device affects its reliability. Also, because the inputs are in the threshold region, the outputs tend to oscillate, resulting in damage to the internal circuit over a long period of time. The data sheet shows the increase in supply current (ΔI_{CC}) when the input is at a TTL level [for ABT V_I = 3.4 V, ΔI_{CC} = 1.5 mA (see Figure 5)]. This becomes more critical when the input is in the threshold region as seen in Figure 6.

These characteristics are typical for all CMOS input circuits, including microprocessors and memories.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
ΔI_{CC}†	ABT	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,		1.5	mA
	LVT	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,		0.2	mA
	LVC, ALVC, LV				0.5	

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Figure 5. Supply Current Change of the Input at TTL Level as Specified in Data Sheets

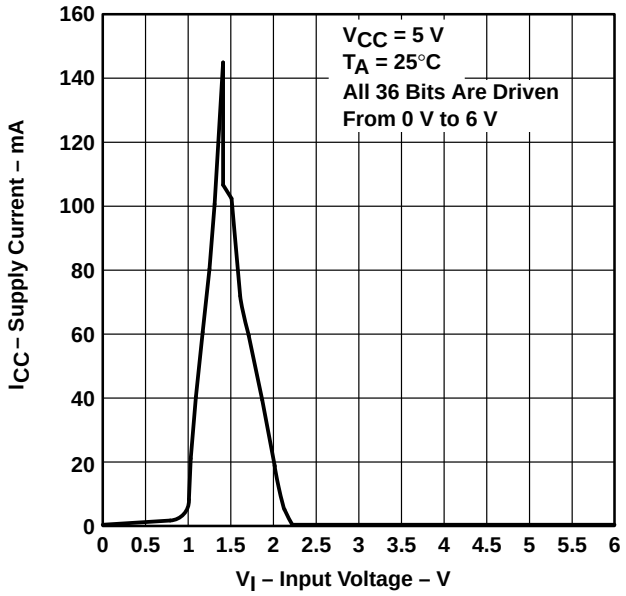

Figure 6. Supply Current Versus Input Voltage (36 Inputs)

As long as the driver is active in a transmission path or bus, the receiver's input is always in a valid state. No input specification is violated as long as the rise and fall times are within the data sheet limits. However, when the driver is in a high-impedance state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus. Figure 7 is an example of a typical bus system. When all transceivers are inactive, the bus line levels are undefined. When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*. The result is a considerable increase in power consumption and a risk of damaging all components on the bus. Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.

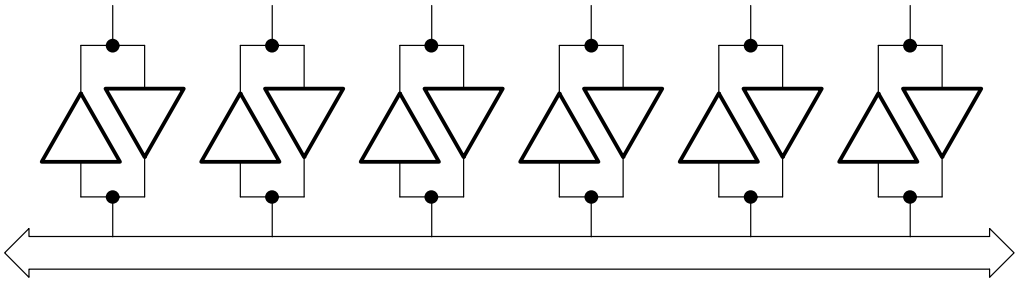

Figure 7. Typical Bidirectional Bus

Recommendations for Designing More Reliable Systems

Bus Control

The simplest way to avoid floating inputs in a bus system is to ensure that the bus is either always active or inactive for a limited time when the voltage buildup does not exceed the maximum V_{IL} specification (0.8 V for TTL-compatible input). At this voltage, the corresponding I_{CC} value is too low and the device operates without any problem or concern (see Figures 2 and 4).

To avoid damaging components, the designer must know the maximum time the bus can float. First, assuming that the maximum leakage current is I_{OZ} = 50 µA and the total capacitance (I/O and line capacitance) is C = 20 pF, the change in voltage with respect to time on an inactive line that exceeds the 0.8-V level can be calculated as in equation 1.

$$\Delta V/\Delta t = \frac{I_{OZ}}{C} = \frac{50\ \mu A}{20\ pF} = 2.5\ V/\mu s \quad (1)$$

The permissible floating time for the bus in this example should be reduced to 320 ns maximum, which ensures that the bus will not exceed the 0.8-V level specified above. The time constant does not change when multiple components are involved because their leakage currents and capacitances are summed.

The advantage of this method is that it requires no additional cost for adding special components. Unfortunately, this method does not always apply because buses are not always active.

Pullup or Pulldown Resistors

When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components from being damaged or overheated. A pullup or a pulldown resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and if its resistance is not chosen properly, a problem may occur. Usually, a 1-kΩ to 10-kΩ resistor is recommended. The maximum input transition time must not be violated when selecting pullup or pulldown resistors (see Figure 3). Otherwise, components may be destroyed.

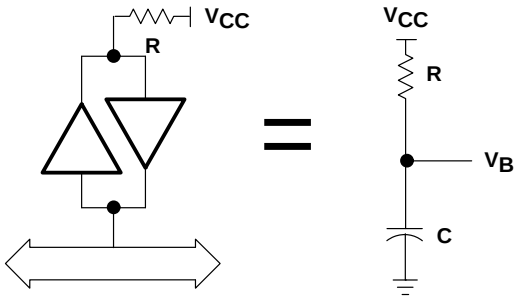

Figure 8. Inactive Bus Model With a Defined Level

Assume that an active-low bus goes to the high-impedance state as modeled in Figure 8. C represents the device plus the bus line capacitance and R is a pullup resistor to V_{CC}. The value of the required resistor can be calculated as in equation 2.

$$V_B = V_{CC}(1 - e^{-t/RC}) \quad (2)$$

Where:

V_B = 0.8 V, maximum allowable floating voltage
V_{CC} = 5 V
C = total capacitance
R = pullup resistor
t = maximum input rise time as specified in Figure 3 of the data sheet

Solving for R, the equation becomes:

$$R = \frac{t}{0.17 \times C} \quad (3)$$

For multiple transceivers on a bus:

$$R = \frac{t}{0.17 \times C \times N} \quad (4)$$

Where:

N = number of components connected to the bus

Assuming that there are ten components connected to the bus, each with a capacitance C = 20 pF requiring a maximum rise time of 10 ns/V, t = 50-ns total rise time for 5-V input, maximum resistor size can be calculated:

$$R = \frac{50\ ns}{0.17 \times 20\ pF \times 10} = 1.5\ k\Omega \quad (5)$$

This pullup resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is very critical. Instead, use the bus-hold feature that is discussed in the next section. The overall advantage of using pullup resistors is that they ensure defined levels when the bus is floating and helps eliminate some of the line reflections because resistors can act as bus terminations as well.

Bus-Hold Circuits

The most effective method to provide defined levels for a floating bus is to use Texas Instruments built-in bus-hold feature on selected families or as an external component like the SN74ACT1071 and SN74ACT1073 (refer to Table 1).

Table 1. Devices With Bus Hold

DEVICE TYPE	BUS HOLD INCORPORATED
SN74ACT1071	10-bit bus hold with clamping diodes
SN74ACT1073	16-bit bus hold with clamping diodes
ABT Widebus+™ (32 and 36 Bit)	All devices
ABT Octals and Widebus™	Selected devices only
Low Voltage (LVT and ALVC)	All devices
LVC Widebus™	All devices

Bus hold is a circuit used in Texas Instruments selected families to help solve the floating input problem and eliminate the need for pullup and pulldown resistors. It consists of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 9). In order to understand how the bus-hold cell operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor. The current requirement of the bus hold is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.

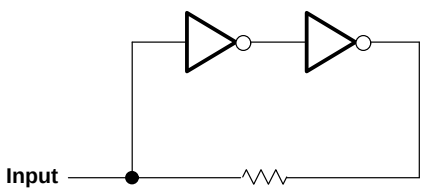

Figure 9. Typical Bus-Hold Cell

As mentioned earlier in this section, Texas Instruments offers the bus hold as stand-alone 10-bit and 16-bit devices (SN74ACT1071 and SN74ACT1073) with clamping diodes to V_{CC} and GND for added protection against line reflections caused by impedance mismatch on the bus. Because purely ohmic resistors cannot be implemented easily in CMOS circuits, a configuration known as a transmission gate is used as the feedback element (see Figure 10). An n channel and a p channel are arranged in parallel between the input and the output of the buffer stage. The gate of the n-channel transistor is connected to V_{CC} and the gate of the p channel is connected to GND. When the output of the buffer is high, the p channel is on, and when the output is low, the n channel is on. Both channels are of relatively small surface area — the on resistance from drain to source, R_{dson}, is about R = 5 kΩ.

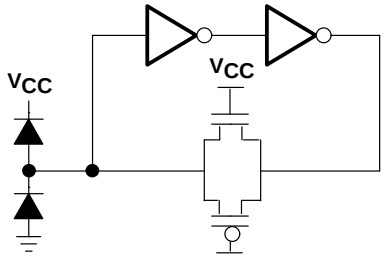

Figure 10. Stand-Alone Bus-Hold Cell (SN74ACT107x)

Now, assume that in a practical application the leakage current of a driver on a bus is I_{OZ} = 10 μA and the voltage drop across the 5 kΩ is V_D = 0.8 V (this value is assumed to ensure a defined logic level). Then, the maximum number of components that a bus hold can handle is calculated as follows:

$$N = \frac{V_D}{I_{OZ} \times R} = \frac{0.8\ V}{10\ \mu A \times 5\ k\Omega} = 16\ \text{components} \quad \textbf{(6)}$$

The 74ACT1071 and 74ACT1073 also provide clamping diodes as an added feature to the bus hold. These diodes are useful for clamping any overshoot or undershoot generated by line reflections. Figure 11 shows the characteristics of the diodes when the input voltage is above V_{CC} or below GND. At V_I = –1V, the diode can source about 50 mA, which can help eliminate undershoots. This can be very useful when noisy buses are a concern.

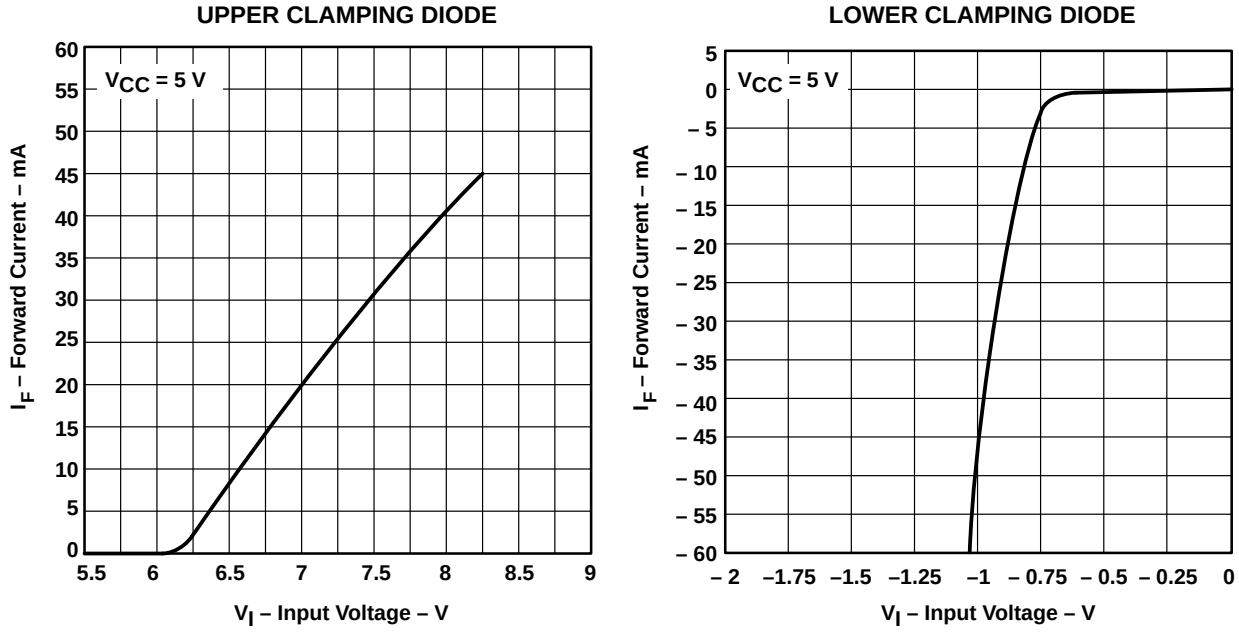

Figure 11. Diode Characteristics (SN74ACT107x)

Texas Instruments also offers the bus-hold circuit as a feature added to some of the advanced-family drivers and receivers. This circuit is similar to the stand-alone circuit with a diode added to the drain of the second inverter (ABT and LVT only, see Figure 12). The diode blocks the overshoot current when the input voltage is higher than V_{CC} ($V_I > V_{CC}$), so only the leakage current is present. This circuit uses the device's input stage as its first inverter; a second inverter creates the feedback feature. The calculation of the maximum number of components that the bus hold can handle is similar to the previous example. However, the advantage of this circuit over the stand-alone bus hold is that it eliminates the need for external components or resistors that occupy more area on the board. This becomes very critical for some designs, especially when wide buses are used. Also, because cost and board-dimension restrictions are a major concern, designers prefer the easy fix: drop-in replaceable parts. Texas Instruments offers this feature in most of the commonly used functions in several families (refer to Table 1 for more details).

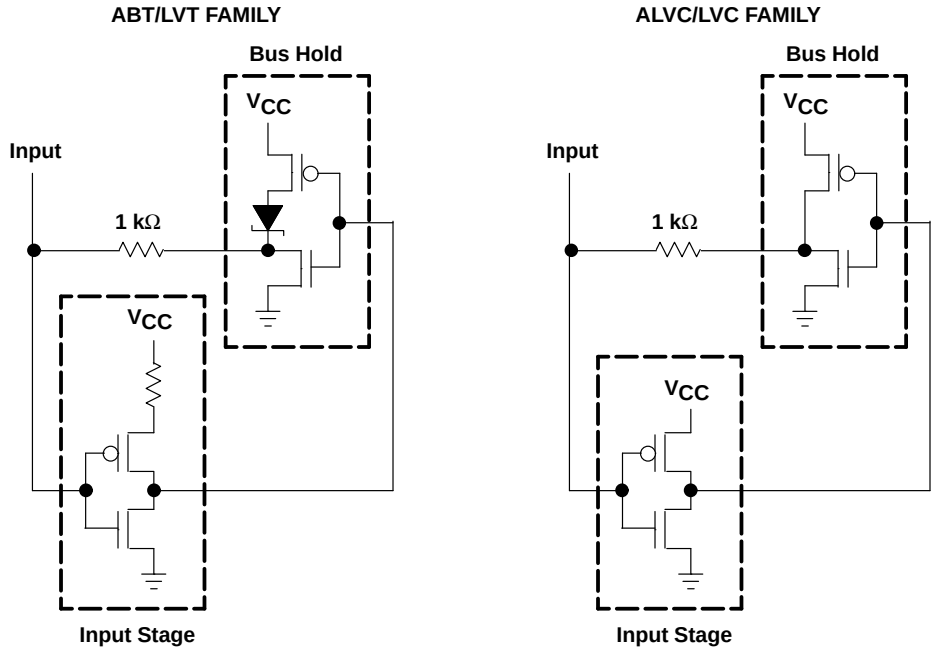

Figure 12. Input Structure of ABT/LVT and ALVC/LVC Families With Bus Hold

Figure 13 shows the input characteristics of the bus hold at 3.3-V and 5-V operations, as the input voltage is swept from 0 to 5 V. These characteristics are similar in behavior to a weak driver. This driver sinks current into the part when the input is low and sources current out of the part when the input is high. When the voltage is near the threshold, the circuit tries to switch to the other state, always keeping the input at a valid level. This is the result of the internal feedback circuit. The plot also shows that the current is at its maximum when the input is near the threshold. $I_{I(hold)}$ maximum is approximately 25 μA for 3.3-V input and 400 μA for 5-V input.

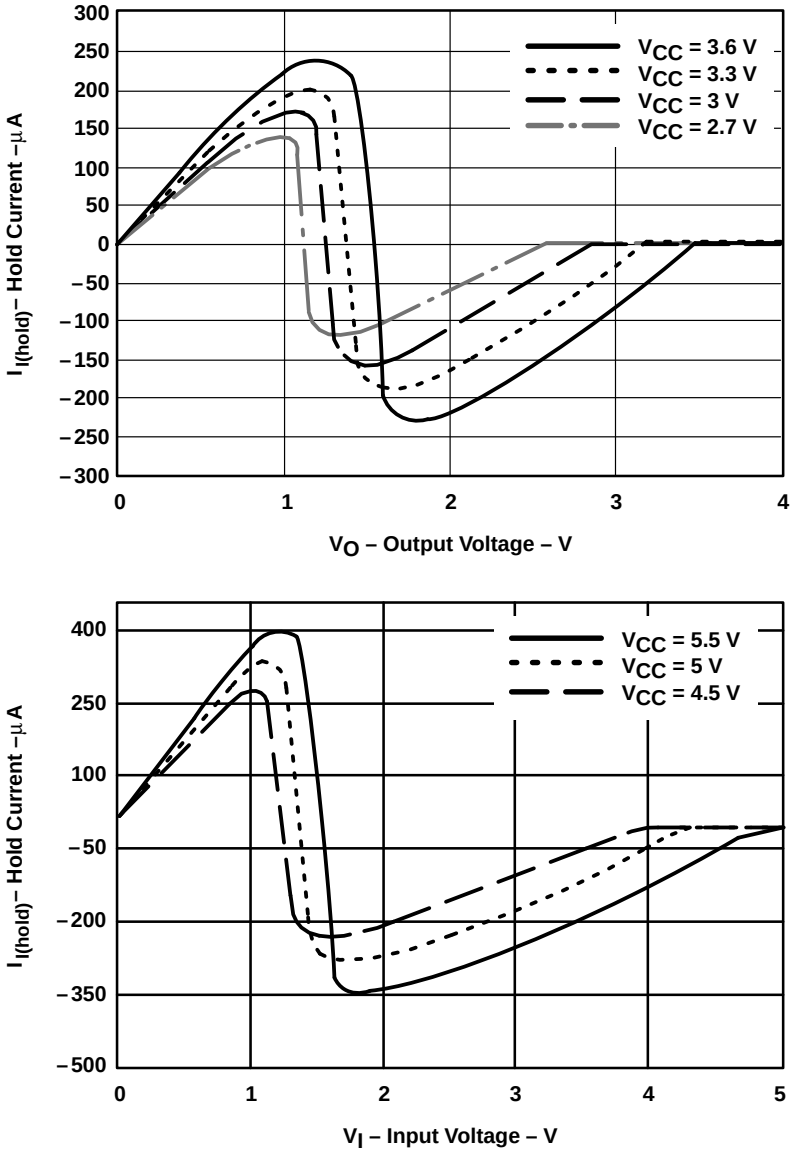

Figure 13. Bus-Hold Input Characteristics

When multiple devices with bus hold are driven by a single driver, one may be concerned about the ac switching capability of the driver becoming weaker. As small drivers, bus-hold cells require an ac current to switch them. This current is not significant when using Texas Instruments CMOS and BiCMOS families. Figure 14 shows a 4-mA buffer driving six LVT16244 devices. The trace is a 75-Ω transmission line. The receivers are separated by 1cm with the driver located in the center of the trace. Figure 15 shows the bus-hold loading effect on the driver when connected to six receivers switching low or high. It also shows the same system with the bus hold disconnected from the receivers. Both plots show the effect of bus hold on the driver's rise and fall times. Initially, the bus hold tries to counteract the driver, causing the rise or fall time to increase. Then, the bus hold changes states (note the crossover point), which helps the driver switch faster, decreasing the rise or fall time.

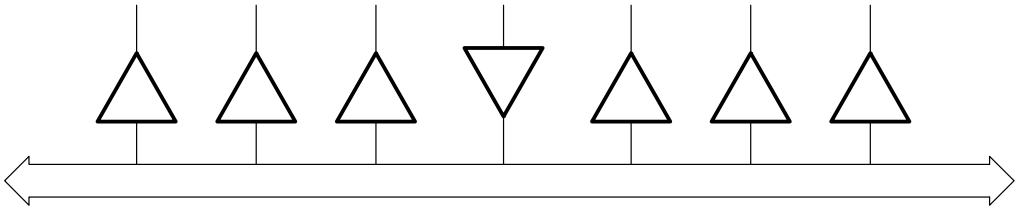

Figure 14. Driver and Receiver System

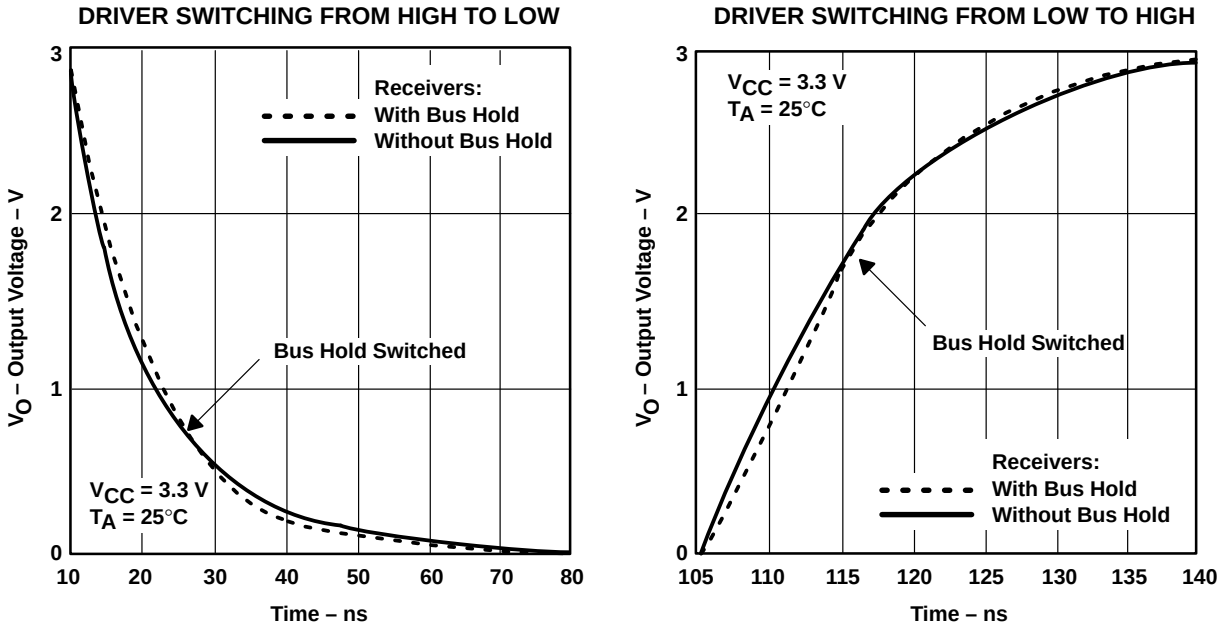

Figure 15. Output Waveforms of the Driver With or Without the Receiver's Bus Hold

Figure 16 shows the supply current (I_{CC}) of the bus-hold circuit as the input is swept from 0 to 5 V. Again, the spike seen at about 1.5-V V_I is due to both the n channel and the p channel conducting simultaneously. This is one of the CMOS transistor characteristics.

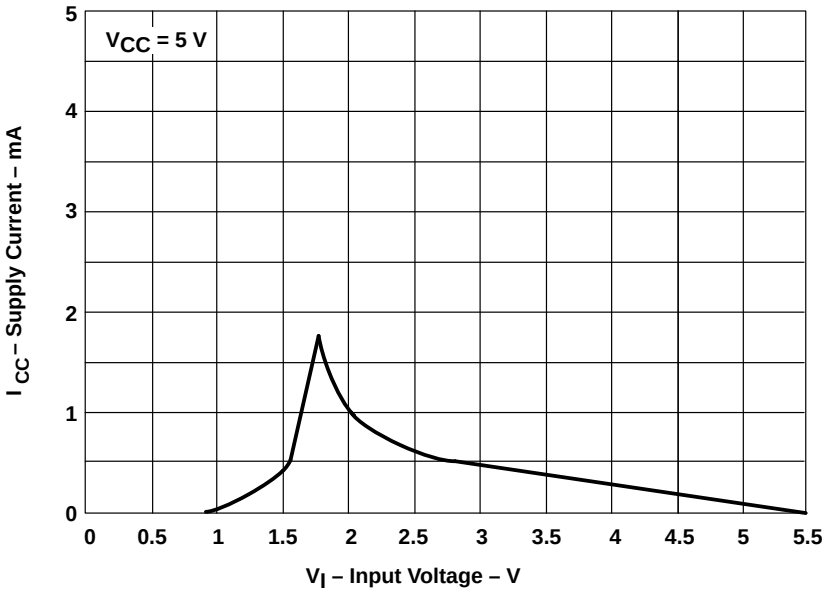

Figure 16. Bus-Hold Supply Current Versus Input Voltage

The power consumption of the bus hold is minimal when switching the input at higher frequencies. Figure 17 shows the power consumed by the input at different frequencies with or without bus hold. As can be seen, the increase in power consumption of the bus hold at higher frequencies is not significant enough to be considered in power calculations.

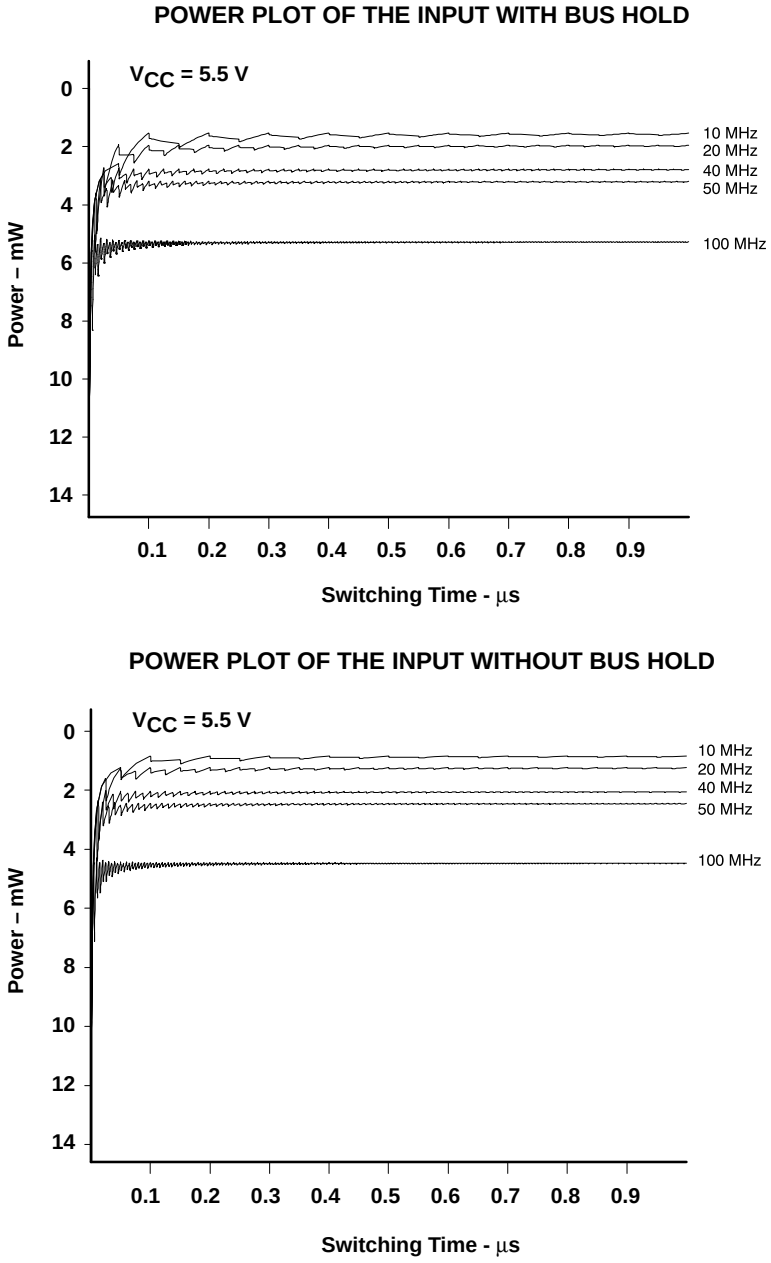

Figure 17. Input Power With or Without Bus Hold at Different Frequencies

Figure 18 shows the data sheet dc specifications for bus hold. The first test condition is the minimum current required to hold the bus at 0.8 V or 2 V. These voltages meet the specified low and high levels for TTL inputs. The second test condition is the maximum current that the bus hold sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input voltage approaches the rail voltage. The output leakage currents, I_{OZH} and I_{OZL}, are insignificant for transceivers with bus hold because a true leakage test cannot be performed due to the existence of the bus-hold circuit. Because bus hold behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with bus hold only and does not apply to buffers. All LVT, ABT Widebus+™, and selected ABT octal and Widebus™ devices have the bus-hold feature (refer to Table 1 or the or contact the local Texas Instruments sales office for more information).

electrical characteristics over recommended operating free-air temperature range (for families with bus-hold feature)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
$I_{I(hold)}$	Data inputs or I/Os	LVT, LVC, ALVC	V_{CC} = 3 V	V_I = 0.8 V	75		µA
				V_I = 2 V	–75		
			V_{CC} = 3.6 V,	V_I = 0 to 3.6 V		±500	
		ABT Widebus+™ and selected ABT Widebus™	V_{CC} = 4.5 V	V_I = 0.8 V	100		
				V_I = 2 V	–100		
			V_{CC} = 5.5 V,	V_I = 0 to 5.5 V		±500	
I_{OZH}/I_{OZL}	Transceivers with bus hold	ABT	This test is not a true I_{OZ} test since bus hold is always active on an I/O pin. It tends to supply a current that is opposite in direction to the output leakage current.			±1	µA
		LVT, LVC, ALVC					
	Buffers with bus hold	ABT	This test is a true I_{OZ} test since bus hold does not exist on an output pin.			±10	
		LVT, LVC, ALVC				±5	

Figure 18. Data Sheet Minimum Specification for Bus Hold

Summary

Floating inputs and slow rise and fall times are important issues to consider when designing with CMOS and advanced BiCMOS families. It is important to understand the complications associated with floating inputs. Terminating the bus properly plays a major role in achieving reliable systems. All three methods that were recommended in this application note should be considered. If it is not possible to control the bus directly and adding pullup or pulldown resistors is impractical due to power-consumption and board-space limitations, bus hold is the best choice. Texas Instruments designed bus hold to reduce the need for resistors used in bus designs, reducing the number of components on the board and improving the overall reliability of the system.