Next-Generation Futurebus+/BTL Transceivers Allow Single-Sided SMT Manufacturing

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Contents

List of Illustrations

Introduction

Futurebus+ (IEEE 896.2-1991) and BTL (IEEE 1194.1-1991) designs offer significant performance advantages over conventional TTL backplane implementations, but these advantages come with trade-offs. Switching noise in the form of ground bounce and EMI must be controlled, and proper termination schemes must be employed to ensure signal integrity in this high-speed switching environment. Trade-offs for price in the form of total system solution versus overall system performance are also of concern. This paper begins with the historical perspective on signal-integrity issues addressed by the IEEE bodies cited above and follows with new pioneering bus-interface solutions to help reduce overall Futurebus+ or BTL system costs and design complexities.

Current Generation of Futurebus+/BTL Transceivers

A number of suppliers have developed Futurebus+ and BTL transceiver solutions that comply with the previously cited IEEE standards. These devices share the same reduced output swing and tight switching thresholds shown in Figure 1 and a slew-rate control (see Figure 2). The various devices differ considerably in wafer-fab process technology, propagation-delay performance, and other performance metrics (see Table 1).

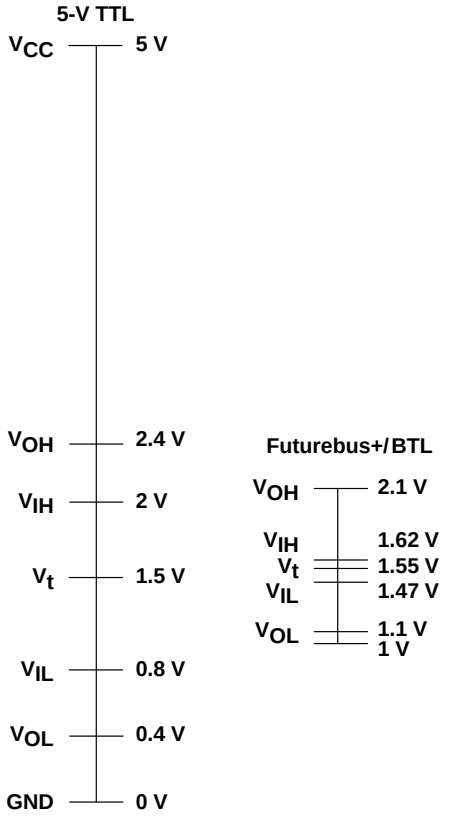


Figure 1. Comparison of TTL and BTL Switching Standards

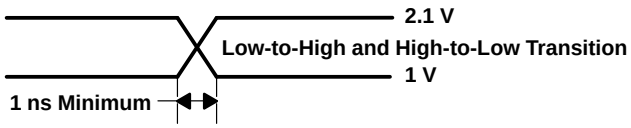


Figure 2. Slew-Rate Control (OEC™) Diagram

Table 1 shows an evolutionary progression in bipolar wafer-fab technology and improved propagation-delay performance. Bipolar fab technologies are chosen for this class of device for their high-drive capability, low switching noise, and relative ease of designing (relative to pure CMOS) the pseudoanalog circuitry required to meet the slew-rate control requirement (see Figure 2). Bipolar circuits have the disadvantage of relatively high power dissipation. The heat generated by this high power dissipation, coupled with the large switching currents coming from the bus termination, place a thermal limitation on the numbers of bits that can be integrated into a single standard integrated-circuit package (typically, only four bits).

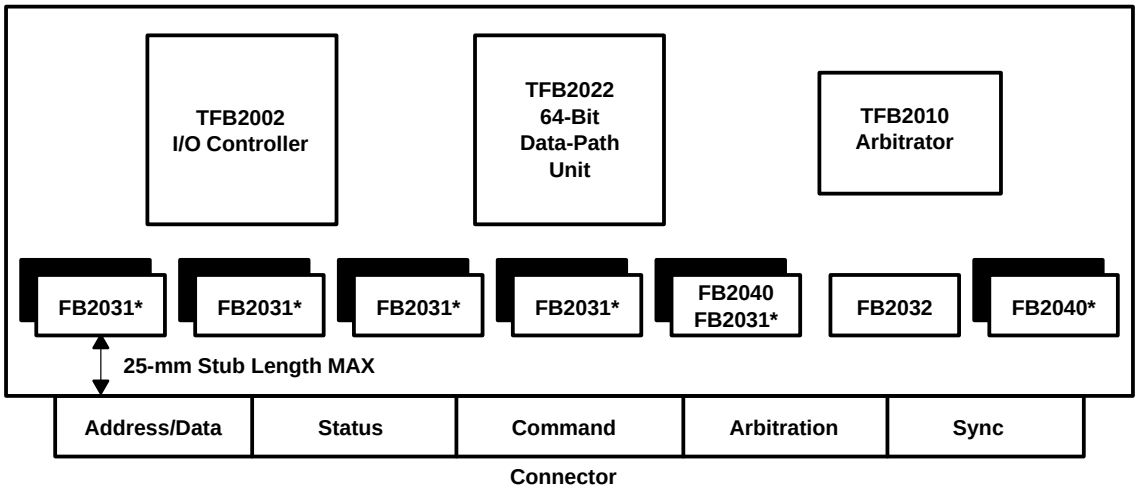
Table 1. Futurebus+/BTL Transceiver Offering Available Today

TRANSCEIVER	SUPPLIER	TECHNOLOGY	BITS/PACKAGE	t_{pd} (ns)
ALS056/057	TI, NSC	3 μ Bipolar	4/8	20
DS3890	NSC	2 μ Bipolar	8†	15
DS3896/7	NSC	1.5 μ Bipolar	4/8	12
DS3893A	NSC	1.2 μ Bipolar	4	7
FB2031/40	TI, Philips	0.8 μ BiCMOS	8/9	6

† Unidirectional driver only; not a true bidirectional transceiver

The newer class of BiCMOS transceivers employs a bipolar output structure to achieve the desired drive, noise, and slew-rate control of previous-generation products. They also offer higher performance, much lower power dissipation, and take the next step toward higher integration (eight or nine bits). However, even this level of density and performance is not totally sufficient for some emerging 128-bit applications. At nine bits, the devices are at the thermal-limit capabilities of the packages, even with low-power BiCMOS technology.

Futurebus+ (IEEE 896.2-1991) adds an additional constraint to board layout by mandating that all compliant cards have a maximum stub length of 25 mm to reduce loading and minimize reflections. This is also a wise rule of thumb for non-Futurebus+/BTL designs. As data paths have increased in width from 32 to 64 bits (128 bits in the future), this stub-length requirement has forced system designers to wrestle with the manufacturing problems of double-sided surface mounting of the transceivers on boards as large as 12 Standard Units (12SU). Even with the relatively dense packaging of today's fastest and most integrated transceivers, this can be a formidable design problem that adds significantly to the overall manufacturing cost of a board (see Figure 3).



NOTE: The second-part type descriptor (*) indicates that a second transceiver is mounted on the opposite side of the board.

Figure 3. Uncached 64-Bit Futurebus+ Layout With Texas Instruments Controller Chipset and Today's Most Integrated Transceivers

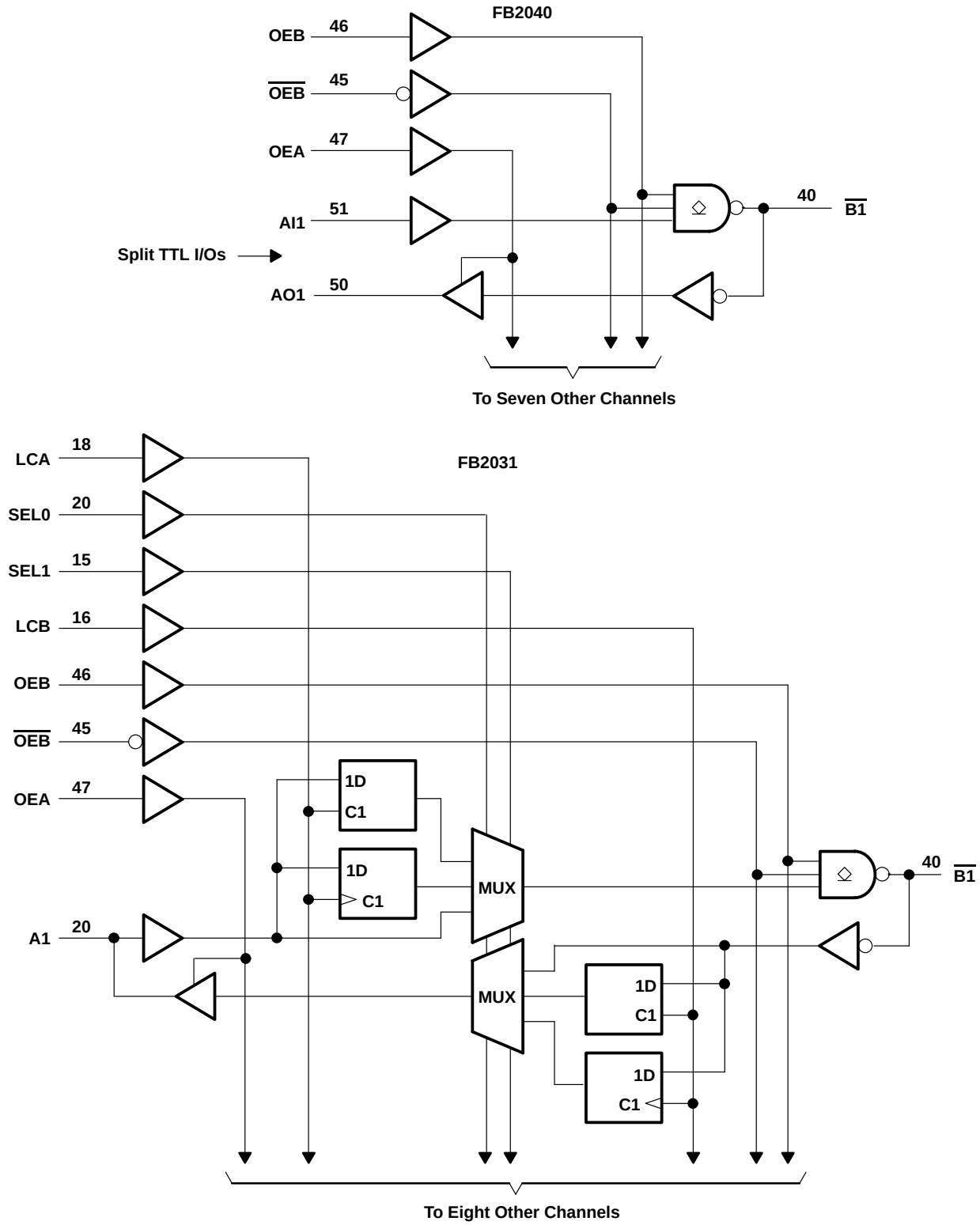
Another problem with the present generation of transceivers is the purchasing requirement for multiple transceiver types. Continuing with the above example, the common 64-bit uncached solution requires three different transceiver types for a complete distributed arbitration Futurebus+ implementation (see Table 2).

Table 2. Transceiver Descriptions for 64-Bit Uncached Futurebus+ Boards Using FB20xx Series Transceivers

DEVICE	DESCRIPTION	QUANTITY PER BOARD	COST EACH IN 1K QUANTITY ($)
FB2031	9-Bit Data/Address Transceiver With Clock and Latch	9	7.95
FB2032†	Arbitration Contest Transceiver	1	9.75
FB2040	8-Bit Status/Sync Transceiver With Split TTL I/O	3	8.10
	Total Part Count and Cost:	13	105.60

† Optional for distributed arbitration only

These transceivers were designed quite differently from one another due to the specific functions they perform in the system (data/address, sync, arbitration, status, or command). Figure 4 highlights the functional differences between the FB2040 (status and sync transceiver) and the FB2031 (address/data transceiver). The main distinctions are the universal storage modes (transparent, latched, or clocked) of the FB2031 and the separate, or split, TTL I/O pins of the FB2040. As previously noted, until recently, efforts to develop any sort of true universal Futurebus+/BTL transceiver have not been practical due to the absence of a viable, high-power, fine-pitch package with more than 56 pins.



Pin numbers shown are for the RC package.

Figure 4. Functional Differences Between FB2040 Control Transceiver and FB2031 Address/Data Transceiver

A New Generation of Futurebus+/BTL Transceivers

In response to the need for single-sided surface mounting and simplified transceiver architectures, Texas Instruments has developed both a high-power package and a series of 18-channel Futurebus+/BTL universal bus transceivers (UBT™). These new devices, designated as the FB16xx series, are packaged in a high-power version of the EIAJ standard 100-pin TQFP package (0.5-mm lead pitch). A package cross section, as shown in Figure 5, reveals a metal heatsink that facilitates the excellent thermal performance of the package.

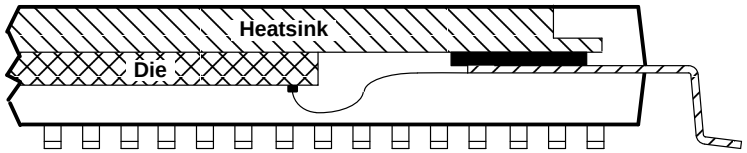
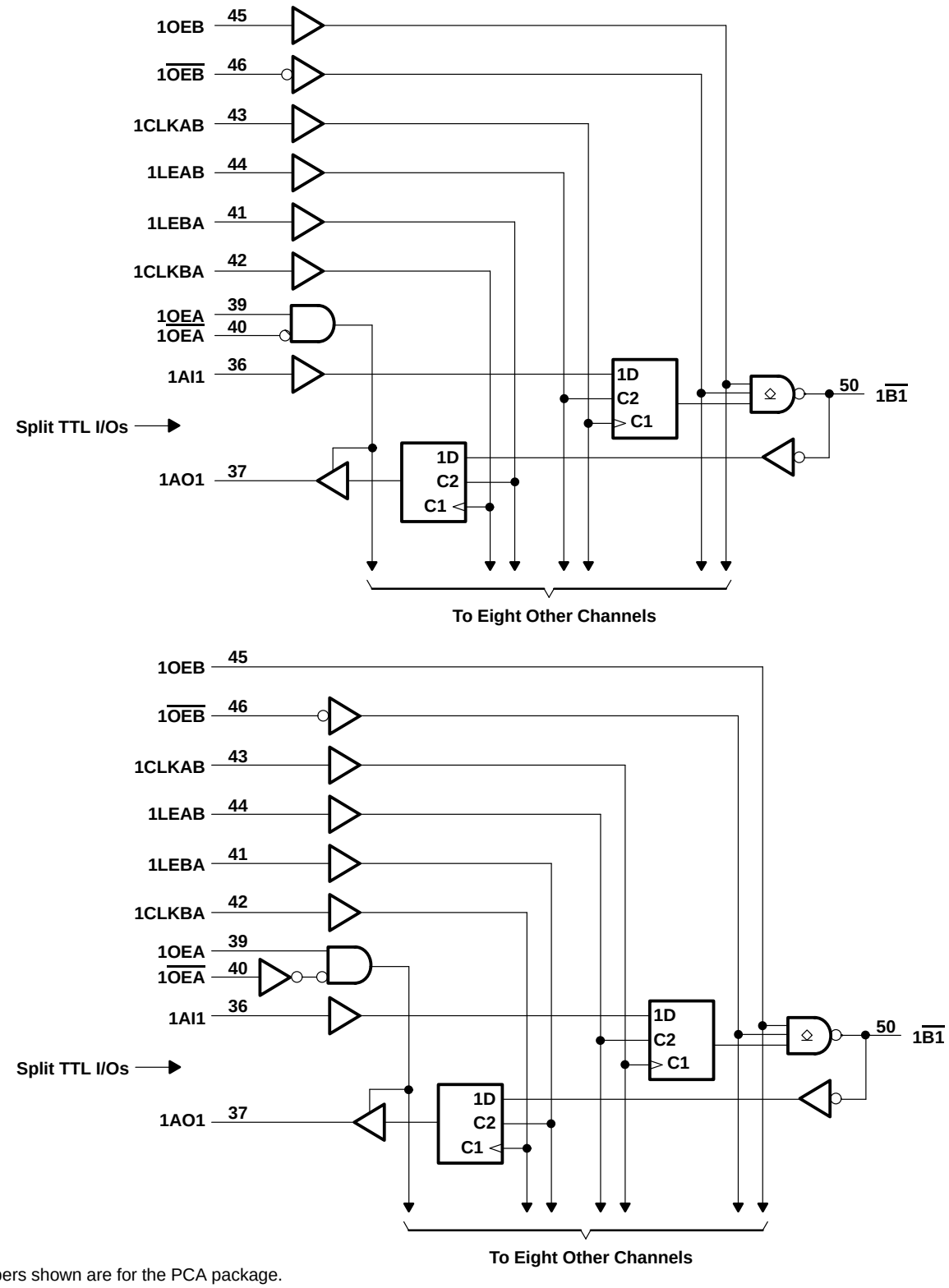


Figure 5. Cross Section of Thermally Enhanced EIAJ 100-Pin TQFP

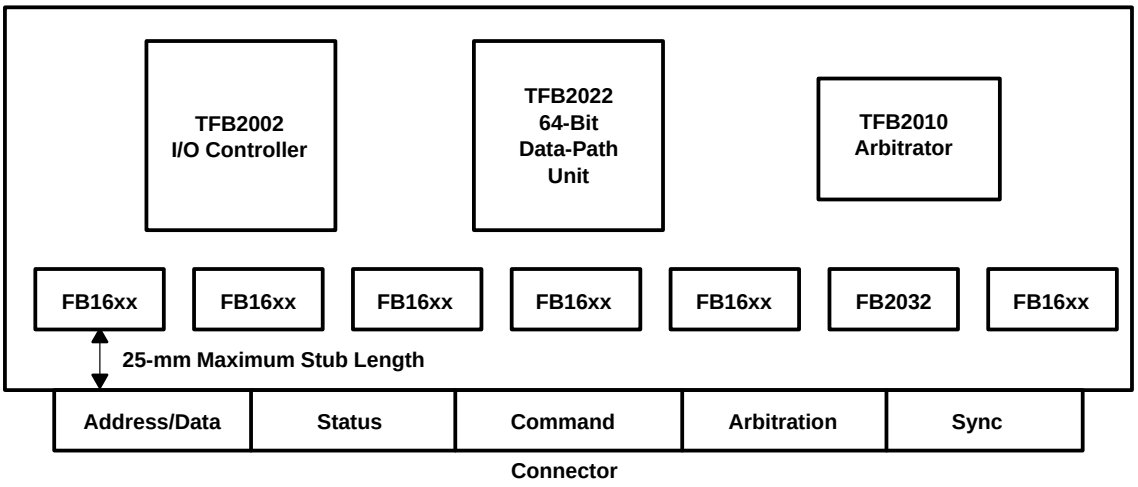
The FB16xx series devices are designed with both the universal data-storage capabilities of the FB2031 address/data transceiver and the separate TTL I/O of the FB2040 control transceiver. This series of devices can be configured as two independent 9-channel transceivers (see Figure 6) or one coherent 18-channel transceiver.



Pin numbers shown are for the PCA package.

Figure 6. Functional Circuit Diagram of FB1650

This flexible design approach eliminates the need for double-sided surface mounting, along with all of the associated manufacturing costs, and still meets the IEEE 896.2-1991 25-mm maximum-stub-length requirement (see Figure 7).



NOTE: There is no double-sided SMT requirement.

Figure 7. Uncached 64-Bit Futurebus+ Layout With Texas Instruments Chipset and FB16xx Transceivers

In addition, the 18-channel architecture lends itself naturally to reduced pin-to-pin signal skew. Advanced BiCMOS circuit design techniques have improved propagation-delay performance over the previous generation of BiCMOS transceivers. Table 3 shows a transceiver cost comparison for the same 64-bit uncached Futurebus+ example considered previously.

Table 3. Cost Comparison for 64-Bit Uncached Futurebus+ Board Using FB16xx Series Transceivers

DEVICE	DESCRIPTION	QUANTITY PER BOARD	COST EACH IN 1K QUANTITY ($)
FB16xx	18-Bit TTL/BTL UBT With Split TTL I/O	6	13.85
FB2032†	Arbitration Contest Transceiver	1	9.75
	Total Part Count and Cost:	7	92.85

† Optional for distributed arbitration only

This is a nearly 50% reduction in component count and a 14% cost savings ($12.75/board) on the transceivers alone. Significant savings (tens of dollars per board) in manufacturing costs are also realized by moving to single-sided SMT manufacturing. Other members of the FB16xx family include system clock-distribution features that lend themselves to more specific end-system applications such as ATM hubs and routers (see Table 4).

Table 4. Transceiver Descriptions for Other Members of the FB16xx Series

DEVICE	DESCRIPTION
FB1650	18-Bit TTL/BTL UBT With Split TTL I/O
FB1651	17-Channel UBT With Separate Buffered and Delayed Clock Bit
FB1652	17-Channel UBT With Separate Buffered Clock Bit (no delay line)

Summary

The high-speed data-communication requirements of today's fastest board-level computers and telecommunications and network switching equipments can be met with Futurebus+ and BTL-compatible transceivers and switching levels. Stub-length constraints and ever-increasing data-path widths have made it difficult to control signal integrity and manufacturing and procurement costs in these high-performance systems. The next generation of 18-channel Futurebus+/BTL universal bus transceivers meets this market need by facilitating low-cost single-sided surface-mount manufacturing, and single-device-type procurement, characterization, qualification, and specification.