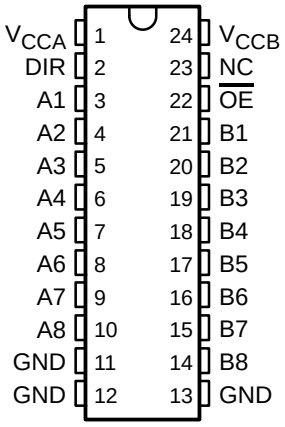
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

**DB, DW, OR PW PACKAGE**
**(TOP VIEW)**




## description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The A port has $V_{CCA}$, which is set at 5 V, and the B port is designed to track $V_{CCB}$, which accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74LVCC4245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVCC4245 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

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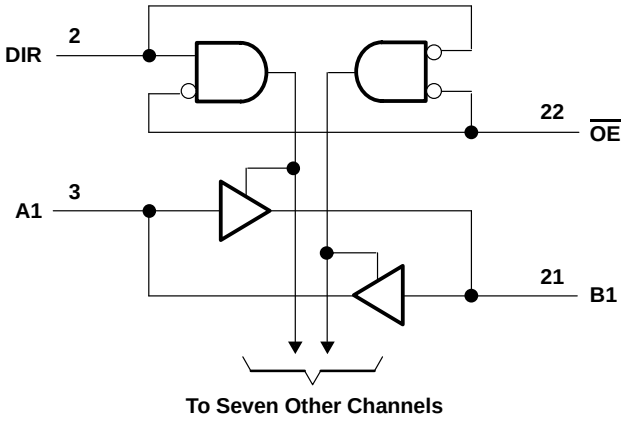
### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CCA}$ and $V_{CCB}$ . . . . . –0.5 V to 6 V
Input voltage range, $V_I$ (see Note 1): I/O ports . . . . . –0.5 to $V_{CC}$ + 0.5 V
Except I/O ports . . . . . –0.5 to $V_{CCA}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CCA}$, $V_{CCB}$, or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 104°C/W
DW package . . . . . 81°C/W
PW package . . . . . 120°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 2)

| | | | | $V_{CCA}$ | $V_{CCB}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | | | 4.5 | 5 | 5.5 | V |
| $V_{CCB}$ | Supply voltage | | | | | 2.7 | 3.3 | 5.5 | V |
| $V_{IHA}$ | High-level input voltage | $V_O \le 0.1$ V, | $V_O \ge V_{CCA} - 0.1$ V | 4.5 V | 2.7 V | 2 | | | V |
| | | | | | 3.6 V | 2 | | | |
| | | | | 5.5 V | 5.5 V | 2 | | | |
| $V_{IHB}$ | High-level input voltage | $V_O \le 0.1$ V, | $V_O \ge V_{CCB} - 0.1$ V | 4.5 V | 2.7 V | 2 | | | V |
| | | | | | 3.6 V | 2 | | | |
| | | | | 5.5 V | 5.5 V | 3.85 | | | |
| $V_{ILA}$ | Low-level input voltage | $V_O \le 0.1$ V, | $V_O \ge V_{CCA} - 0.1$ V | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | | | 3.6 V | | | 0.8 | |
| | | | | 5.5 V | 5.5 V | | | 0.8 | |
| $V_{ILB}$ | Low-level input voltage | $V_O \le 0.1$ V, | $V_O \ge V_{CCB} - 0.1$ V | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | | | 3.6 V | | | 0.8 | |
| | | | | 5.5 V | 5.5 V | | | 1.65 | |
| $V_{IA}$ | Input voltage | | | | | 0 | | $V_{CCA}$ | V |
| $V_{IB}$ | Input voltage | | | | | 0 | | $V_{CCB}$ | V |
| $V_{OA}$ | Output voltage | | | | | 0 | | $V_{CCA}$ | V |
| $V_{OB}$ | Output voltage | | | | | 0 | | $V_{CCB}$ | V |
| $I_{OHA}$ | High-level output current | | | 4.5 V | 3 V | | | –12 | mA |
| | | | | 5 V | 3 V | | | –24 | |
| $I_{OHB}$ | High-level output current | | | 5 V | 2.7 V | | | –12 | mA |
| | | | | | 3 V | | | –24 | |
| $I_{OLA}$ | Low-level output current | | | 4.5 V | 3 V | | | 12 | mA |
| | | | | 5 V | 3 V | | | 24 | |
| $I_{OLB}$ | Low-level output current | | | 5 V | 2.7 V | | | 12 | mA |
| | | | | | 3 V | | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | | | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | | | | –40 | | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

PRODUCT PREVIEW

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OHA}$ | | $I_{OH}$ = –100 μA | 4.5 V | 3 V | 4.4 | 4.49 | | V |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3 V | 3.76 | 4.25 | | |
| $V_{OHB}$ | | $I_{OH}$ = –100 μA | 4.5 V | 3 V | 2.25 | 2.65 | | V |
| | | $I_{OH}$ = –12 mA | 4.5 V | 2.7 V | 2.2 | 2.5 | | |
| | | | | 3 V | 2.46 | 2.85 | | |
| | | $I_{OH}$ = –24 mA | 4.5 V | 2.7 V | 2 | 2.1 | | |
| | | | | 3 V | 2.25 | 2.65 | | |
| | | | | 4.5 V | 3.76 | 4.25 | | |
| $V_{OLA}$ | | $I_{OL}$ = 100 μA | 4.5 V | 3 V | | | 0.1 | V |
| | | $I_{OL}$ = 24 mA | 4.5 V | 3 V | | 0.21 | 0.44 | |
| $V_{OLB}$ | | $I_{OL}$ = 100 μA | 4.5 V | 3 V | | | 0.1 | V |
| | | $I_{OL}$ = 12 mA | 4.5 V | 2.7 V | | 0.11 | 0.44 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | 2.7 V | | 0.22 | 0.5 | |
| | | | | 3 V | | 0.21 | 0.44 | |
| | | | | 4.5 V | | 0.18 | 0.44 | |
| $I_I$ | Control pins | $V_I = V_{CCA}$ or GND | 5.5 V | 3.6 V | | ±0.1 | ±1 | μA |
| | | | | 5.5 V | | ±0.1 | ±1 | |
| $I_{OZ}$† | A or B ports | $V_O = V_{CC}$ or GND, $V_I = V_{IL}$ or $V_{IH}$ | 5.5 V | 3.6 V | | ±0.5 | ±5 | μA |
| $I_{CCA}$ | B to A | $A_n = V_{CC}$ or GND | 5.5 V | Open | | 8 | 80 | μA |
| | | $A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND | 5.5 V | 3.6 V | | 8 | 80 | |
| | | | | 5.5 V | | 8 | 80 | |
| $I_{CCB}$ | A to B | $A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND | 5.5 V | 3.6 V | | 5 | 50 | μA |
| | | | | 5.5 V | | 8 | 80 | |
| $\Delta I_{CCA}$‡ | A port | $\overline{V_I} = V_{CCA} - 2.1$ V, Other inputs at $V_{CCA}$ or GND, $\overline{OE}$ at GND and DIR at $V_{CCA}$ | 5.5 V | 5.5 V | | 1.35 | 1.5 | mA |
| | $\overline{OE}$ | $V_I = V_{CCA} - 2.1$ V, Other inputs at $V_{CCA}$ or GND, DIR at $V_{CCA}$ or GND | 5.5 V | 5.5 V | | 1 | 1.5 | |
| | DIR | $\overline{V_I} = V_{CCA} - 2.1$ V, Other inputs at $V_{CCA}$ or GND, $\overline{OE}$ at $V_{CCA}$ or GND | 5.5 V | 3.6 V | | 1 | 1.5 | |
| $\Delta I_{CCB}$‡ | B port | $\overline{V_I} = V_{CCB} - 0.6$ V, Other inputs at $V_{CCB}$ or GND, $\overline{OE}$ at GND and DIR at $V_{CCB}$ | 5.5 V | 3.6 V | | 0.35 | 0.5 | mA |
| $C_i$ | Control inputs | $V_I = V_{CCA}$ or GND | Open | Open | | 4.5 | | pF |
| $C_{io}$ | A or B ports | $V_O = V_{CCA}$ or GND | 5 V | 3.3 V | | 10 | | pF |

† For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CCB}$.

**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCA}$ = 5 V ± 0.5 V, $V_{CCB}$ = 5 V ± 0.5 V | | | $V_{CCA}$ = 5 V ± 0.5 V, $V_{CCB}$ = 2.7 V TO 3.6 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP‡ | MAX | |
| $t_{PHL}$ | A | B | 1 | 4.9 | 7 | 1 | 5.5 | 8 | ns |
| $t_{PLH}$ | | | 1 | 4 | 6 | 1 | 5 | 7.5 | |
| $t_{PHL}$ | B | A | 1 | 4.7 | 7 | 1 | 5.6 | 8 | ns |
| $t_{PLH}$ | | | 1 | 3.9 | 5.5 | 1 | 4.3 | 6.5 | |
| $t_{PZL}$ | $\overline{OE}$ | A | 1 | 7.4 | 10 | 1 | 8 | 11 | ns |
| $t_{PZH}$ | | | 1 | 6.1 | 8.5 | 1 | 6.3 | 8 | |
| $t_{PZL}$ | $\overline{OE}$ | B | 1 | 5.6 | 8 | 1 | 6.7 | 10 | ns |
| $t_{PZH}$ | | | 1 | 5.7 | 8 | 1 | 6.9 | 10 | |
| $t_{PLZ}$ | $\overline{OE}$ | A | 1 | 2.9 | 5 | 1 | 2.9 | 5.5 | ns |
| $t_{PHZ}$ | | | 1 | 3.4 | 6 | 1 | 3.4 | 6 | |
| $t_{PLZ}$ | $\overline{OE}$ | B | 1 | 3.8 | 6 | 1 | 4.2 | 7 | ns |
| $t_{PHZ}$ | | | 1 | 4.8 | 7.5 | 1 | 6 | 9.5 | |
| $t_{sk(o)}$§ | Data or output | Output | | 1 | 1.5 | | 1 | 1.5 | ns |

† Typical values are at $T_A$ = 25°C, $V_{CCA}$ = 5 V, and $V_{CCB}$ = 5 V.
‡ Typical values are at $T_A$ = 25°C, $V_{CCA}$ = 5 V, and $V_{CCB}$ = 3.3 V.
§ Skew is the difference in the propagation delay of any two outputs of the same device. This parameter is ensured by design.

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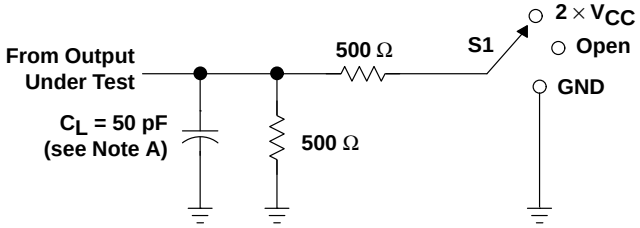
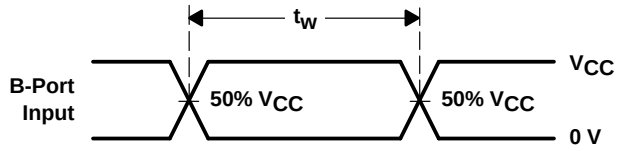
## PARAMETER MEASUREMENT INFORMATION FOR B PORT (SEE NOTE E)

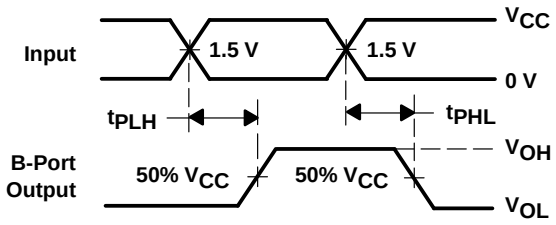



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open |

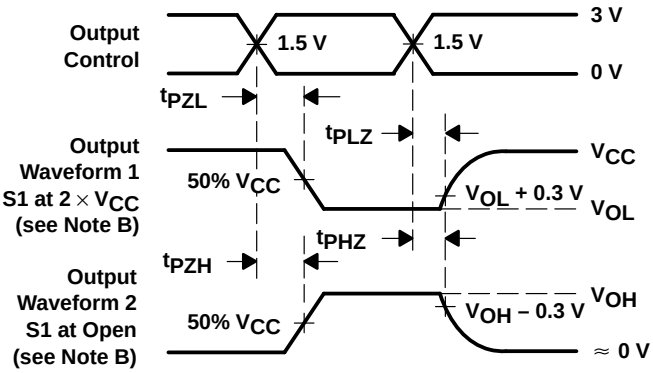
LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



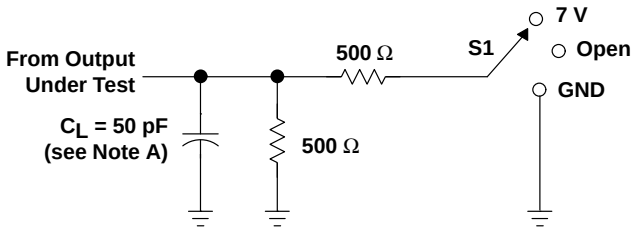

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. This is to test the B port, with $V_{CCA}$ = 5.5 V and $V_{CCB}$ = 5.5 V.

**Figure 1. Load Circuit and Voltage Waveforms**

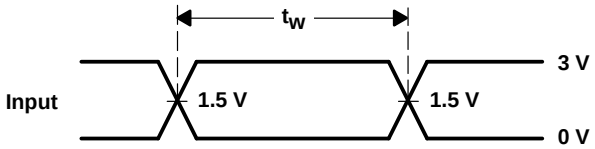
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT (SEE NOTE E)

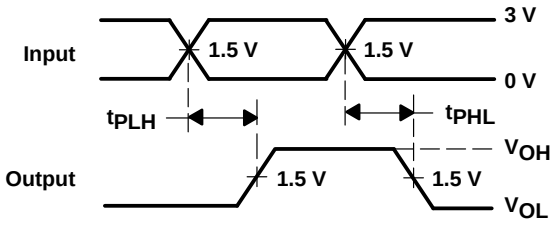



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

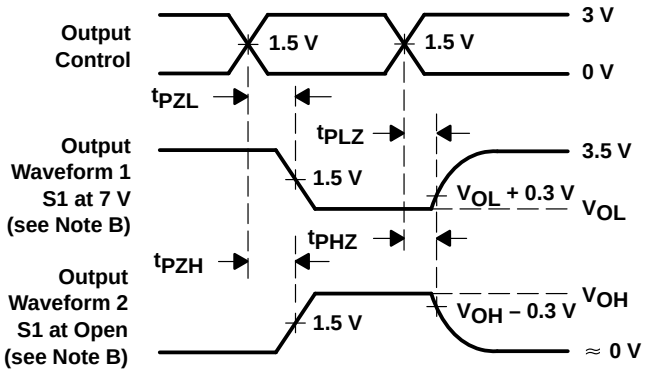
LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. This is to test the A and B ports, with $V_{CCA}$ = 5.5 V and $V_{CCB}$ = 3.6 V.

**Figure 2. Load Circuit and Voltage Waveforms**

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