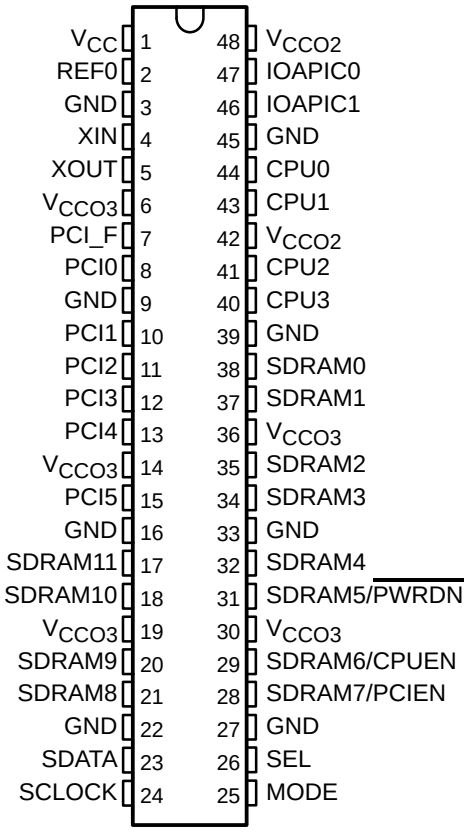
- **Clock Generation for Intel 440LX Chipset**
- **Four CPU Clock Outputs With Programmable Frequency**
- **Twelve SDRAM Clock Outputs**
- **Seven PCI Clock Outputs**
- **One 14.318-MHz Reference Clock Output**
- **All Output Clock Frequencies Derived From a Single 14.31818-MHz Crystal Input**
- **Internal Loop Filter for Phase-Lock Loop (PLL)**
- **Selectable Desktop or Mobile Function**

DL PACKAGE
(TOP VIEW)



description

The CDC9441 is a system clock synthesizer for use in personal computer systems utilizing the Intel 440LX chipset. An integrated crystal oscillator generates a 14.318-MHz reference frequency, while an integrated PLL generates a selectable CPU clock frequency from a 14.31818-MHz crystal input.

The CDC9441 provides four 2.5-V copies of the CPU clock, 12 3.3-V copies of the CPU frequency for use by SDRAM, seven 3.3-V copies of one-half the CPU frequency for PCI, two 2.5-V copies of the 14.318-MHz clock for APIC use, and one 3.3-V copy of the 14.318-MHz output for use as an ISA reference clock.

CPU output frequencies are selectable to either 60 MHz or 66.67 MHz. The output frequency is determined by the SEL control input. When SEL = L, the nominal CPU clock output frequency is 60 MHz. When SEL = H, the nominal CPU clock output frequency is 66.67 MHz. SEL has an integrated pullup resistor, so the default CPU output frequency is 66.67 MHz.

Two modes of operation are offered, desktop and mobile. The device configuration is selected via the MODE control input. When MODE = H, the device is in the desktop configuration. When MODE = L, the device is in the mobile configuration. In the desktop configuration, pins 31, 29, and 28 are outputs SDRAM5, SDRAM6, and SDRAM7, respectively. However, when in the mobile configuration, pins 31, 29, and 28 are power-down enable ($\overline{\text{PWRDN}}$), CPU clock bank-enable (CPUEN), and PCI bank-enable (PCIEN) inputs, respectively.

The CDC9441 also provides a serial interface bus for additional control of the device. Each output can be individually enabled or disabled by setting the appropriate control bits within the serial bus register space. A PLL bypass (TEST) mode and output 3-state also can be enabled by setting the appropriate bits in the serial bus register space.

The CDC9441 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
CPU(0:3)	41, 41, 43, 44	O	2.5-V CPU clock outputs with programmable frequency. These outputs can be disabled to a logic low by deasserting CPUEN in the mobile mode (i.e., MODE = L).
IOAPIC(0:1)	46, 47	O	2.5 V, 14.318-MHz APIC clock outputs
MODE	25	I	Desktop or mobile mode select. When MODE = H, the device functions in the desktop mode and pins 31, 29, and 28 are outputs SDRAM5, SDRAM6, and SDRAM7, respectively. When MODE = L, the device functions in the mobile mode and pins 31, 29, and 28 are inputs $\overline{\text{PWRDN}}$, CPUEN, and PCIEN, respectively. A 100-kΩ (nominal) pullup resistor is internally integrated so the default is the desktop mode.
PCI_F	7	O	3.3-V free-running PCI clock output at one-half the CPU clock frequency. PCI_F is not disabled via the PCIEN signal.
PCI(0:5)	8, 10, 11, 12, 13, 15	O	3.3-V PCI clock outputs at one-half the CPU clock frequency. These outputs can be disabled to a logic low by deasserting PCIEN in the mobile mode (i.e., MODE = L).
REF0	2	O	3.3 V, 14.318-MHz ISA reference clock output
SCLOCK	24	I	IIC serial clock input
SDATA	23	I/O	IIC serial data input/out
SDRAM(0:4) SDRAM(8:11)	17, 18, 20, 21, 32, 34, 35, 37, 38	O	3.3-V SDRAM clock outputs synchronous and in-phase with the CPU clock outputs.
SDRAM5/$\overline{\text{PWRDN}}$	31	I/O	3.3 V SDRAM clock output or power-down enable input based on the condition of the MODE control input. When MODE = H, this pin functions as a 3.3 V SDRAM clock output. When MODE = L, this pin functions as the $\overline{\text{PWRDN}}$ control input, which can be used to disable all outputs to a low state and place the integrated oscillator and PLL in a static state for low power consumption.
SDRAM6/CPUEN	28	I/O	3.3-V SDRAM clock output or CPU clock bank-enable input based on the condition of the MODE control input. When MODE = H, this pin functions as a 3.3-V SDRAM clock output. When MODE = L, this pin functions as the CPUEN control input, which can be used to enable or disable the CPU clock outputs.
SDRAM7/PCIEN	27	I/O	3.3-V SDRAM clock output or PCI bank-enable input based on the condition of the MODE control input. When MODE = H, this pin functions as a 3.3-V SDRAM clock output. When MODE = L, this pin functions as the PCIEN control input, which can be used to enable or disable the PCI clock outputs, with the exception of PCI_F.
SEL	26	I	Clock frequency select. When SEL = H, the CPU clock power-up frequency is 66.67 MHz. When SEL = L, the CPU clock power-up frequency is 60 MHz. A 100-kΩ (nominal) pullup resistor is internally integrated so the default power-up condition is 66.67 MHz.
XIN	4	I	Crystal input. The oscillator is designed for use with a 50-PPM, 18-pF parallel resonant crystal. A TTL-level clock also can drive this input.
XOUT	5	O	Crystal output.
V_{CC}	1	Power	3.3-V core power supply
V_{CCO2}	42, 48	Power	2.5-V output power supply
V_{CCO3}	6, 14, 19, 30, 36	Power	3.3-V output power supply
GND	3, 9, 16, 22, 27, 33, 39, 45	Ground	Ground

FUNCTION TABLE

MODE	$\overline{\text{PWRDEN}}$	CPUEN	PCIEN	SEL	XIN	CPUn	SDRAMn†	PCI_F	PCIn	REFn	IOAPICn
L	L	X	X	X	14.318 MHz‡	L	L	L	L	L	L
L	H	L	L	L	14.318 MHz	L	60 MHz	30 MHz	L	14.318 MHz	14.318 MHz
L	H	L	L	H	14.318 MHz	L	66.67 MHz	33.33 MHz	L	14.318 MHz	14.318 MHz
L	H	L	H	L	14.318 MHz	L	60 MHz	30 MHz	30 MHz	14.318 MHz	14.318 MHz
L	H	L	H	H	14.318 MHz	L	66.67 MHz	33.33 MHz	33.33 MHz	14.318 MHz	14.318 MHz
L	H	H	L	L	14.318 MHz	60 MHz	60 MHz	30 MHz	L	14.318 MHz	14.318 MHz
L	H	H	L	H	14.318 MHz	66.67 MHz	66.67 MHz	33.33 MHz	L	14.318 MHz	14.318 MHz
L	H	H	H	L	14.318 MHz	60 MHz	60 MHz	30 MHz	30 MHz	14.318 MHz	14.318 MHz
L	H	H	H	H	14.318 MHz	66.67 MHz	66.67 MHz	33.33 MHz	33.33 MHz	14.318 MHz	14.318 MHz
H	NA†	NA†	NA†	L	14.318 MHz	60 MHz	60 MHz	30 MHz	30 MHz	14.318 MHz	14.318 MHz
H	NA†	NA†	NA†	H	14.318 MHz	66.67 MHz	66.67 MHz	33.33 MHz	33.33 MHz	14.318 MHz	14.318 MHz

† Pins 31, 29, and 28 function as inputs $\overline{\text{PWRDN}}$, CPUEN, and PCIEN, respectively, when MODE = L, and as outputs SDRAM5, SDRAM6, and SDRAM7, respectively, when MODE = H.
‡ The allowable reference frequency is minimum = 14.316 MHz, nominal = 14.31818 MHz, and maximum = 14.32 MHz.

PLL-COUNTER VALUES

SELECTED FREQUENCY	M	N	ACTUAL FREQUENCY§	PPM ERROR
60 MHz	21	88	59.9999	0
66.67 MHz	26	121	66.6346	–531

§ Actual frequency based on a 14.31818-MHz input reference frequency

DEVICE CONTROL TABLE

I2C BYTE 0, BIT 1	I2C BYTE 0, BIT 0	DEFINITION
L	L	Normal operation
L	H	Test mode. PLL bypass
H	L	Reserved
H	H	3-state mode; all outputs are placed in a high-impedance state.

I2C BYTE 0-BIT DEFINITION

BIT	DEFINITION	DEFAULT VALUE
7	Reserved	H
6	Reserved	L
5	Reserved	L
4	Reserved	L
3	Reserved	H
2	Reserved	H
1	See device control table	L
0	See device control table	L

PRODUCT PREVIEW

I2C BYTE 1-BIT DEFINITION

BIT	DEFINITION	DEFAULT VALUE
7	Reserved	H
6	Reserved	H
5	Reserved	H
4	Reserved	H
3	CPU3 enable	H
2	CPU2 enable	H
1	CPU1 enable	H
0	CPU0 enable	H

I2C BYTE 2-BIT DEFINITION

BIT	DEFINITION	DEFAULT VALUE
7	Reserved	H
6	PCI_F enable	H
5	PCI5 enable	H
4	PCI4 enable	H
3	PCI3 enable	H
2	PCI2 enable	H
1	PCI1 enable	H
0	PCI0 enable	H

I2C BYTE 3-BIT DEFINITION

BIT	DEFINITION	DEFAULT VALUE
7	SDRAM7 enable	H
6	SDRAM6 enable	H
5	SDRAM5 enable	H
4	SDRAM4 enable	H
3	SDRAM3 enable	H
2	SDRAM2 enable	H
1	SDRAM1 enable	H
0	SDRAM0 enable	H

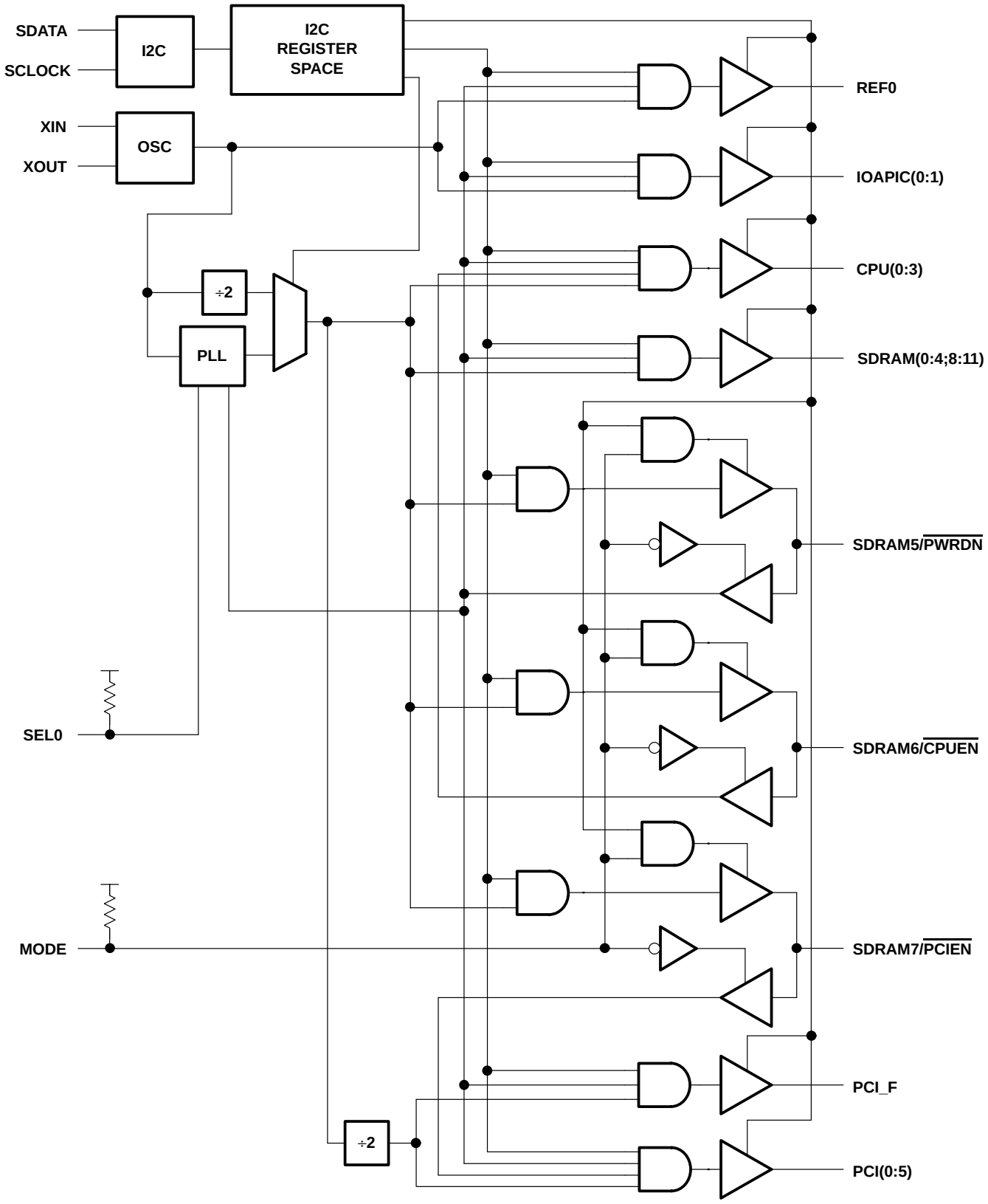
I2C BYTE 4-BIT DEFINITION

BIT	DEFINITION	DEFAULT VALUE
7	Reserved	H
6	Reserved	H
5	Reserved	H
4	Reserved	H
3	SDRAM11 enable	H
2	SDRAM10 enable	H
1	SDRAM9 enable	H
0	SDRAM8 enable	H

I2C BYTE 5-BIT DEFINITION

BIT	DEFINITION	DEFAULT VALUE
7	Reserved	H
6	Reserved	H
5	IOAPIC1 enable	H
4	IOAPIC0 enable	H
3	Reserved	H
2	Reserved	H
1	Reserved	H
0	REF0 enable	H

functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: V_{CC} . . . . . –0.5 V to 4.6 V
V_{CCO2} . . . . . –0.5 V to 3.6 V
V_{CCO3} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . . –0.5 V to V_{CCO} + 0.5 V
Current into any output in the low state, I_O . . . . . 24 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	3.3-V core supply voltage	3.135	3.465	V
V_{CCO2}	2.5-V I/O supply voltage	2.375	2.625	V
V_{CCO3}	3.3-V I/O supply voltage	3.135	3.465	V
V_{IH}	High-level input voltage	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage	–0.3	0.8	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = 3.135 V,	I_I = –18 mA				–1.2	V
V_{OH3}	V_{CCO3} = 3.135 V,	I_{OH} = –1 mA		2.4			V
V_{OL3}	V_{CCO3} = 3.135 V,	I_{OL} = 1 mA				0.4	V
V_{OH2}	V_{CCO2} = 2.375 V,	I_{OH} = –1 mA		2			V
V_{OL2}	V_{CCO2} = 2.375 V,	I_{OL} = 1 mA				0.4	V
I_I	V_{CC} = 3.465 V,	V_I = V_{CC} or GND				±5	µA
I_I (pullup/down)	V_{CC} = 3.465 V,	V_I = V_{CC} or GND				±100	µA
I_{OZ}	V_{CC} = 3.465 V,	V_O = 3.135 V or 0					µA
I_{CC}	V_{CC} = 3.465 V,	I_O = 0, V_I = V_{CC} or GND	Outputs low				mA
			Outputs disabled				
C_i	Except XIN				5		pF
C_o	Except XOUT				6		pF
C_{pd}	V_I = 3.135 V or 0						pF

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
Stabilization time†	After $\overline{\text{PWRDN}}\downarrow$		3	ms
	After power up		3	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN.

switching characteristics, CPU clocks (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
Period‡		CPUn	SEL = H	15		ns
			SEL = L	16.7		
Jitter‡		CPUn			±250	ps
t_r‡§		CPUn		0.4	1.6	ns
t_f‡§		CPUn		0.4	1.6	ns
Duty cycle‡		CPUn		45	55	%
t_{skew}‡	CPUn	CPUn			250	ps
Clock enable latency	CPUEN	CPUn‡		1	4	CPU cycles

‡ Specifications are applicable only after the PLL stabilization time has elapsed.
§ Rise and fall times are characterized using the test circuit shown in Figure 1.

switching characteristics, SDRAM clocks (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
Period‡		SDRAMn	SEL = H	15		ns
			SEL = L	16.7		
Jitter‡		SDRAMn			±250	ps
t_r‡§		SDRAMn		0.4	1.33	ns
t_f‡§		SDRAMn		0.4	1.33	ns
Duty cycle‡		SDRAMn		45	55	%
t_{skew}‡	SDRAMn	SDRAMn			500	ps
Clock enable latency	CPUn	SDRAMn			500	ps

‡ Specifications are applicable only after the PLL stabilization time has elapsed.
§ Rise and fall times are characterized using the test circuit shown in Figure 1.

PRODUCT PREVIEW

switching characteristics, PCI clocks (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
Period†		PCIn	SEL = H	30		ns
			SEL = L	33.4		
Jitter†		PCIn			±500	ps
t_r†‡		PCIn		0.5	2	ns
t_f†‡		PCIn		0.5	2	ns
Duty cycle†		PCIn		45	55	%
t_{skew}†		PCIn			500	ps
$t_{hpoffset}$†	CPUn	PCIn		1	4	ns
Clock enable latency	PCIEN	PCIn†		1	4	CPU cycles

† Specifications are applicable only after the PLL stabilization time has elapsed.
‡ Rise and fall times are characterized using the test circuit shown in Figure 1.

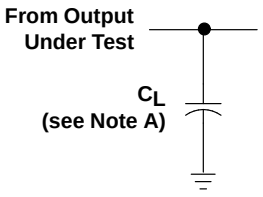
switching characteristics, fixed clocks (REF0, IOAPICn) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_r†‡		REFn	0.5	2	ns
		IOAPICn	0.4	1.6	
t_f†‡		REFn	0.5	2	ns
		IOAPICn	0.4	1.6	

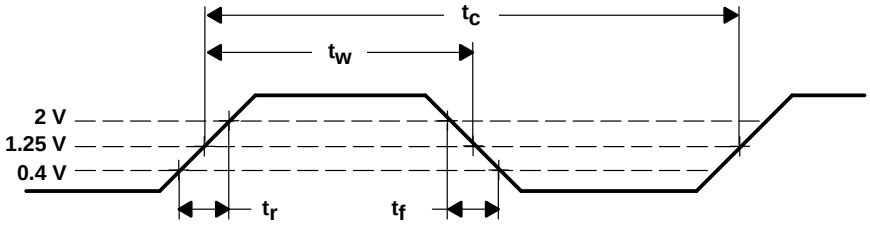
† Specifications are applicable only after the PLL stabilization time has elapsed.
‡ Rise and fall times are characterized using the test circuit shown in Figure 1.

PRODUCT PREVIEW

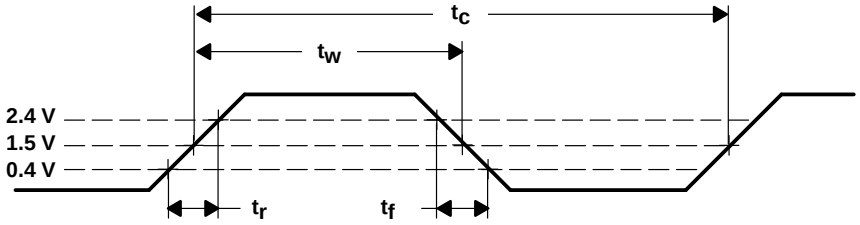
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



2.5-V CLOCK WAVEFORMS



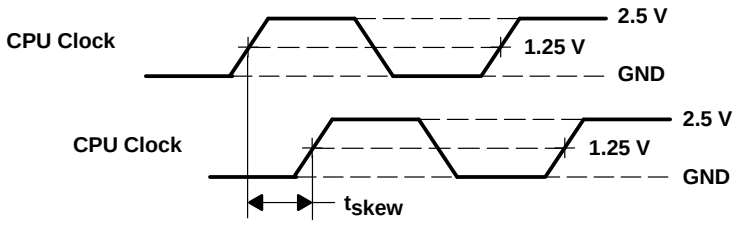
3.3-V CLOCK WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
C_L = 20 pF (CPUn, IOAPICn, REF1)
C_L = 30 pF (PCIn, PCI_F, SDRAMn)
C_L = 45 pF (REF0)
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 W, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. Duty cycle = ($t_w \div t_c$) × 100%

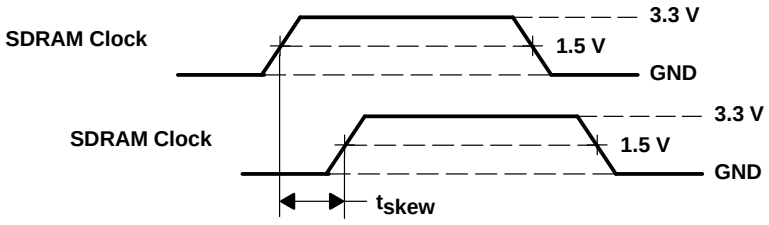
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

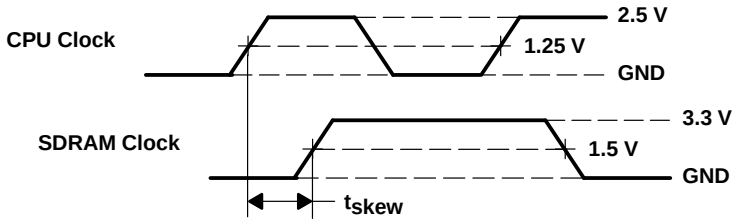
PARAMETER MEASUREMENT INFORMATION



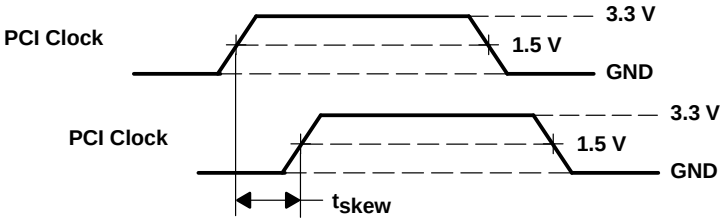
CPU-CLOCK TO CPU-CLOCK SKEW



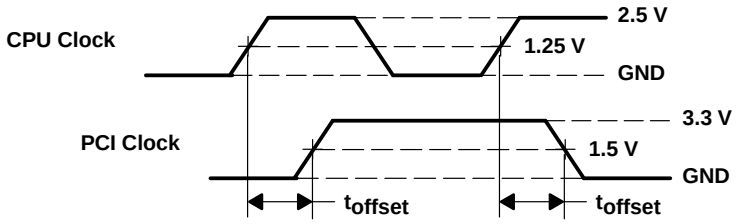
SDRAM-CLOCK TO SDRAM-CLOCK SKEW



CPU-CLOCK TO SDRAM-CLOCK OFFSET



PCI-CLOCK TO PCI-CLOCK SKEW

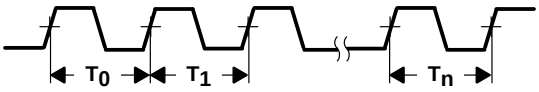


CPU-CLOCK TO PCI-CLOCK OFFSET

Figure 2. Waveforms for Calculation of $t_{sk(o)}$ and $t_{hpoffset}$

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Jitter (cycle-to-cycle) = $T_1 - T_0$
B. Jitter (peak-to-peak) = MAX{T_0:T_n} – MIN{T_0:T_n}

Figure 3. Jitter Measurement

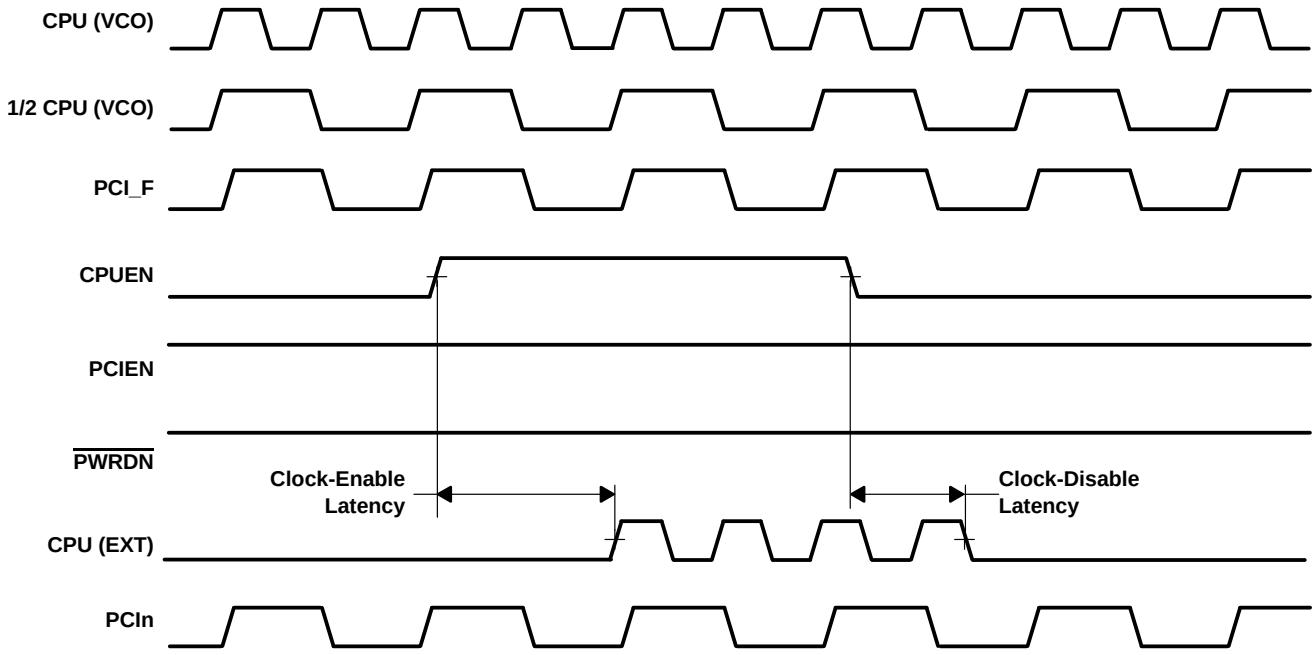


Figure 4. CPU Clock-Enable Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

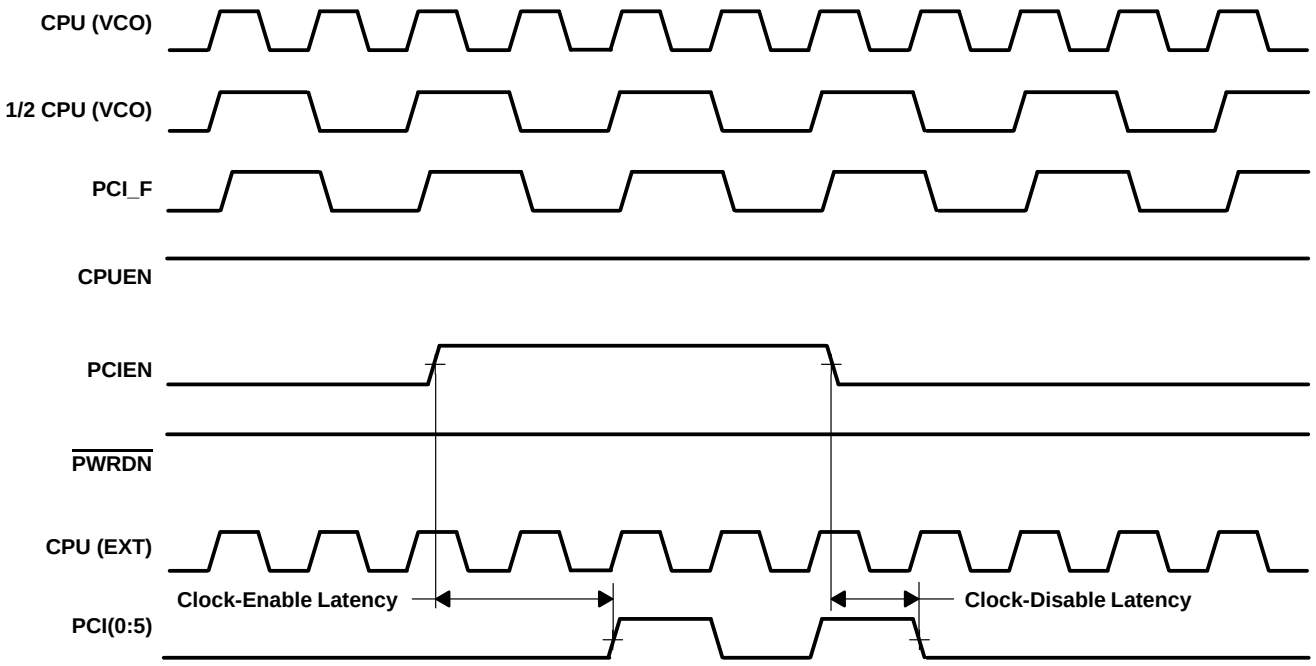


Figure 5. PCI Clock-Enable Timing

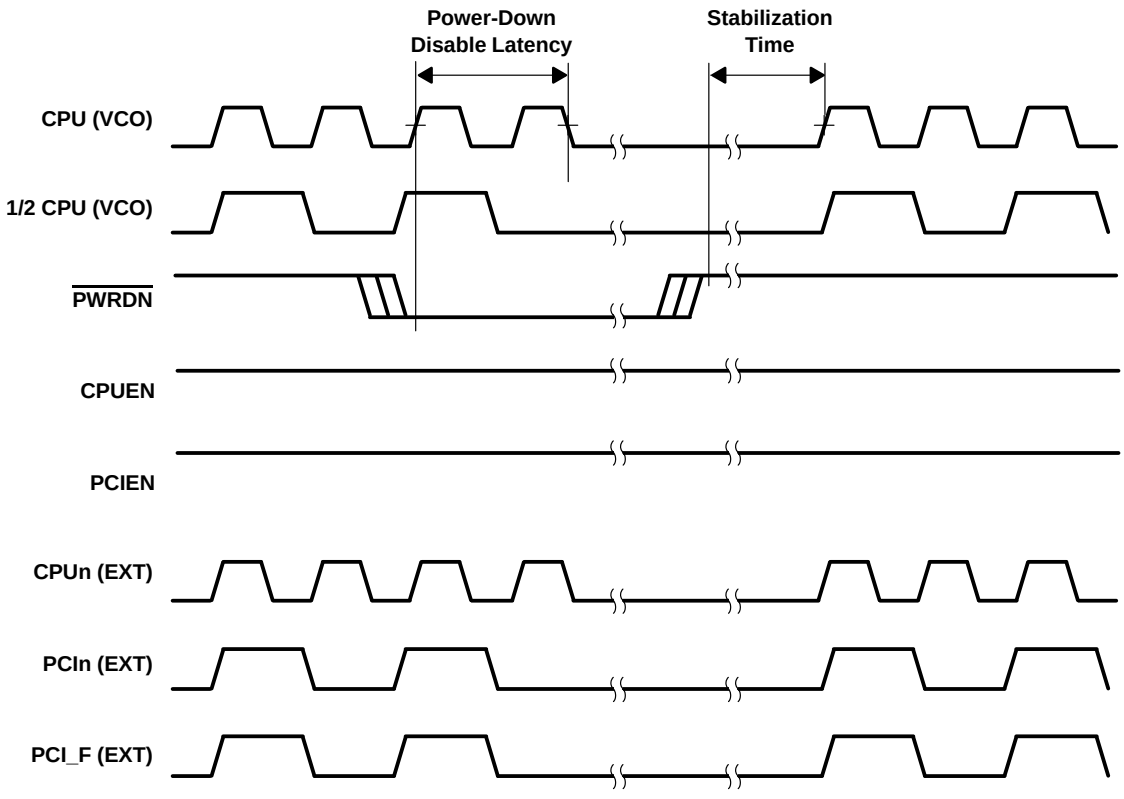


Figure 6. Power-Down Timing

PRODUCT PREVIEW

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