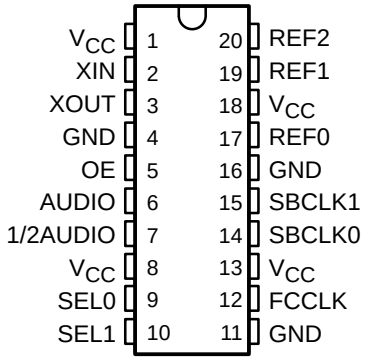
- **Utility Clock Generation for Personal Computer Applications**
- **Two 48-MHz Serial Bus Clock Outputs**
- **One 24-MHz Super I/O Controller Clock Output**
- **One AUDIO Clock Output With Selectable Frequency**
- **One Clock Output at 1/2 AUDIO Clock Frequency**
- **All Output Clock Frequencies Derived From a Single 14.31818-MHz Crystal Input**
- **Internal Loop Filters for Phase-Lock Loops (PLL)**
- **Packaged in Shrink Small-Outline Package**

DB PACKAGE
(TOP VIEW)



description

The CDC9449 is a system clock synthesizer for use in personal computer systems. An integrated crystal oscillator generates a 14.318-MHz reference frequency, while two integrated PLLs generate a 48-MHz clock, a 24-MHz clock, and a selectable AUDIO and 1/2 AUDIO clock frequency from a 14.31818-MHz crystal input.

The CDC9449 provides two copies of the 48-MHz serial bus clock, one copy of the 24-MHz super I/O controller clock, one copy of the AUDIO clock, one copy of the 1/2 AUDIO clock, and three copies of the 14.318-MHz reference frequency.

All outputs are 3-state and can be disabled by the output-enable (OE) control input. When OE = L, all outputs are placed in a high-impedance state.

The CDC9449 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

OE	SEL1	SEL0	XIN†	SBCLKn	FCCLK	REFn	AUDIO	1/2 AUDIO
L	X	X	14.318 MHz	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z
H	L	L	TCLK	TCLK/2	TCLK/4	TCLK	TCLK/2	TCLK/4
H	L	H	14.318 MHz	48 MHz	24 MHz	14.318 MHz	24.576 MHz	12.288 MHz
H	H	L	14.318 MHz	48 MHz	24 MHz	14.318 MHz	33.8688 MHz	16.934 MHz
H	H	H	14.318 MHz	48 MHz	24 MHz	14.318 MHz	L	L

† The allowable reference frequency is minimum = 14.316 MHz, nominal = 14.31818 MHz, and maximum = 14.32 MHz.
‡ TCLK is a test clock driven over XIN in the test mode.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

48-MHz PLL COUNTER VALUES

FREQUENCY	M	N	VCO FREQUENCY†	ACTUAL OUTPUT FREQUENCY	PPM ERROR
48 MHz	17	57	48.0080 MHz	48.0080 MHz	167

† Actual frequency based on a 14.31818-MHz input reference frequency

AUDIO PLL COUNTER VALUES

FREQUENCY	M	N	VCO FREQUENCY†	ACTUAL OUTPUT FREQUENCY	PPM ERROR
24.576 MHz	60	103	24.5795 MHz	24.5795 MHz	144
33.8688 MHz	41	97	33.8688 MHz	33.8680 MHz	–24

† Actual frequency based on a 14.31818-MHz input reference frequency

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
REF(0:2)	17, 19, 20	O	14.318-MHz reference clock outputs
SBCLK(0:1)	14, 15	O	48-MHz serial bus clock outputs
FCCLK	12	O	24-MHz super I/O controller clock output
AUDIO	6	O	Audio clock output with selectable output frequency
1/2 AUDIO	7	O	1/2 audio clock output
SEL(0:1)	9, 10	I	Select control bits. These inputs provide function and frequency control for the device. A nominal 100-kΩ pullup resistor is internally integrated on each input.
OE	5	I	Output enable. Active high; when asserted, all outputs are enabled. When deasserted, all outputs are placed in a high-impedance state. A nominal 100-kΩ pullup resistor is internally integrated.
XIN	2	I	Crystal input. The oscillator is designed for use with a 50-PPM 18-pF parallel resonant crystal. A TTL-level clock also can drive XIN.
XOUT	3	O	Crystal output
V_{CC}	1, 8, 13, 18	Power	3.3-V core power supply
GND	4, 11, 16	Ground	Ground

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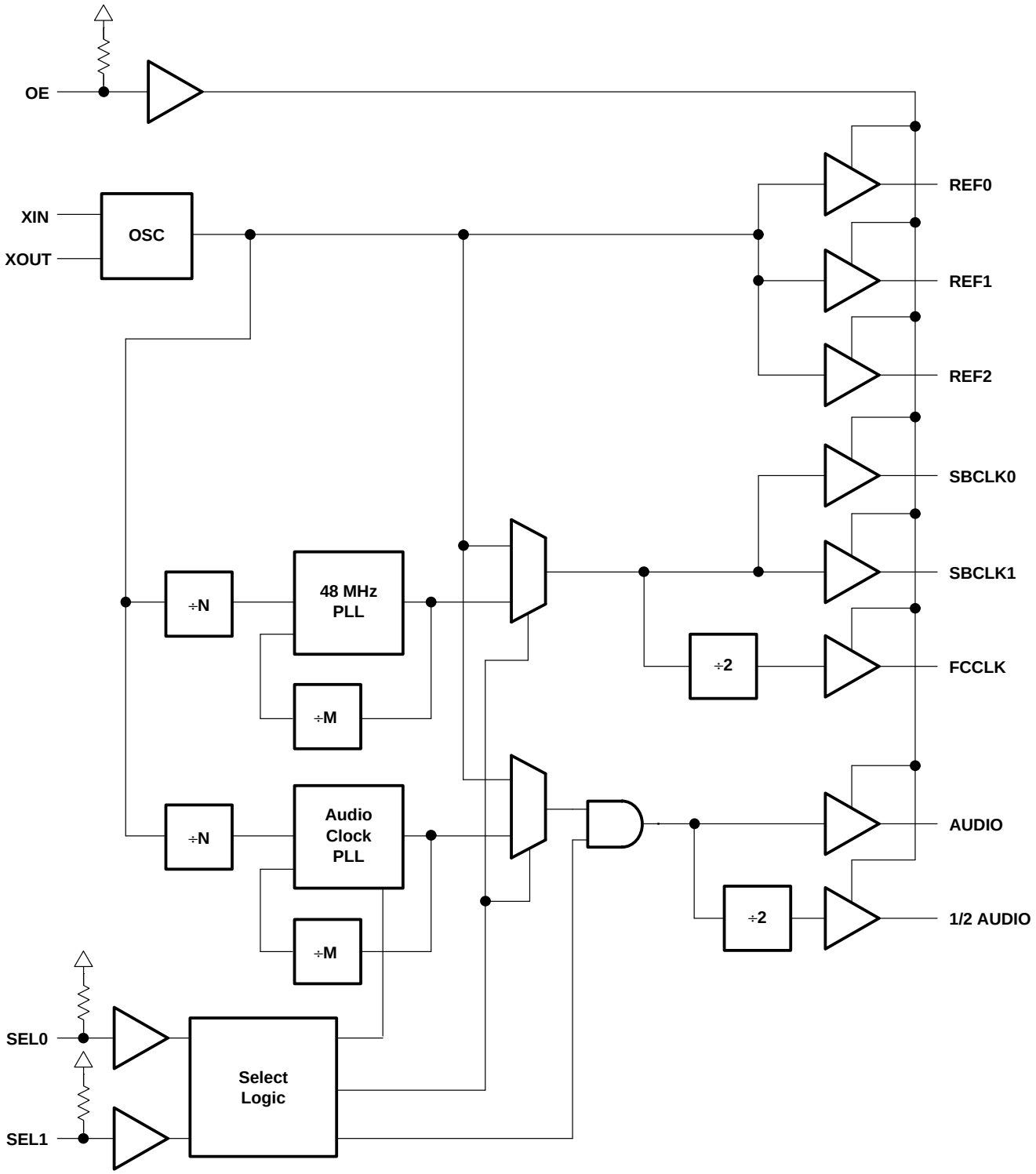
functional block diagram



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V_O
(see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 24 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 0.6 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	3.3-V core supply voltage	3.135	3.465	V
V_{IH}	High-level input voltage	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage	–0.3	0.8	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = 3.135 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 3.135 V,	I_{OH} = –1 mA		2.4			V
V_{OL}	V_{CC} = 3.135 V,	I_{OL} = 1 mA				0.4	V
I_I	V_{CC} = 3.465 V,	V_I = V_{CC} or GND				±5	µA
I_I (pullup/down)	V_{CC} = 3.465 V,	V_I = V_{CC} or GND				±100	µA
I_{OZ}	V_{CC} = 3.465 V,	V_O = 3.135 V or 0					µA
I_{CC}	V_{CC} = 3.465 V,	I_O = 0, V_I = V_{CC} or GND	Outputs low				mA
			Outputs disabled				
C_i	Except XIN				5		pF
C_o	Except XOUT				6		pF
C_{pd}	V_I = 3.135 V or 0						pF

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
Stabilization time†	After power up		3	ms
	After change to SEL(0:1)		3	ms

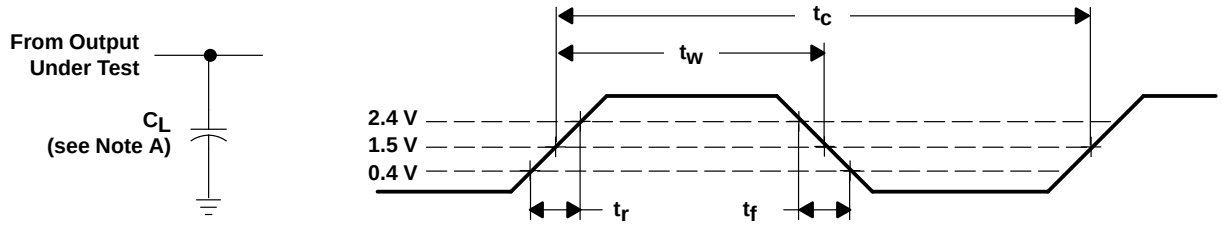
† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN.

switching characteristics (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
Jitter‡		SBCLKn, FCCLK, AUDIO, 1/2 AUDIO		±500	ps
Duty cycle‡		SBCLKn, FCCLK, AUDIO, 1/2 AUDIO	45%	55%	
t_r‡§		Any output	0.5	2	ns
t_f‡§		Any output	0.5	2	ns

‡ Specifications are applicable only after the PLL stabilization time has elapsed.
§ Rise and fall times are characterized using the test circuit shown in Figure 1.

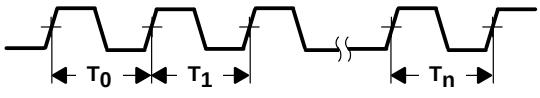
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT **3.3-V CLOCK WAVEFORMS**

NOTES: A. C_L includes probe and jig capacitance.
C_L = 20 pF (SBCLKn, FCCLK, AUDIO, 1/2 AUDIO, REF1, REF2)
C_L = 45 pF (REF0)
B. The outputs are measured one at a time with one transition per measurement.
C. Duty cycle = (t_w t_c) × 100%

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Jitter (cycle-to-cycle) = $T_1 – T_0$
B. Jitter (peak-to-peak) = MAX{T_0:T_n} – MIN{T_0:T_n}

Figure 2. Jitter Measurement

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