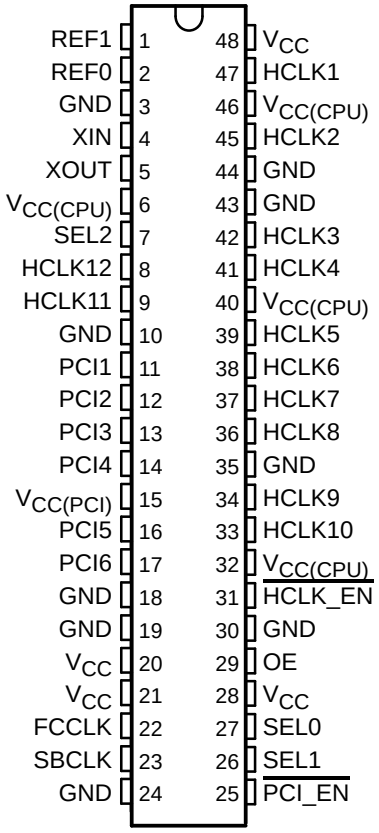
- **Clock Generation for Pentium®/430VX Motherboards**
- **Twelve Host Clock Outputs With Programmable Frequency**
- **Six PCI Clock Outputs**
- **One Serial Bus 48-MHz Clock**
- **One Floppy Controller 24-MHz Clock**
- **Two Reference 14.318-MHz Clock Outputs**
- **All Output Clock Frequencies Derived From a Single 14.31818-MHz Crystal Input**
- **Internal Loop Filters for Phase-Lock Loops (PLLs)**
- **Power-Down Modes**
- **Packaged in Plastic Shrink Small-Outline Package**

DL PACKAGE
(TOP VIEW)



description

The CDC9163 is an integrated clock synthesizer specifically designed for use in Pentium®/430VX based motherboards. Twelve host clock outputs (HCLKn) are programmable via the SEL(0:2) control inputs. This allows four HCLK clocks for use with the processor and chipset, and eight HCLK clocks for use with synchronous DRAM dual in-line memory modules (SDRAM DIMM). The CDC9163 provides six copies of the PCI clock (PCIn), which can be disabled via the $\overline{\text{PCI\_EN}}$ control input. All PCI clocks operate at one-half the host clock frequency, and are offset 1 ns to 4 ns from the rising edge of the host clock. In addition, the CDC9163 generates a 48-MHz serial bus clock (SBCLK), a 24-MHz floppy controller clock, and two copies of the 14.318-MHz reference clock (REFn). All output frequencies are generated from a 14.31818-MHz crystal or oscillator input.

PLLs are used to generate the host clock and serial bus clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components. The PCI clock frequency is derived from the base host clock frequency, while the floppy controller clock is derived from the serial bus clock frequency.

The host and PCI clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs are 3 state and are disabled via the output-enable (OE) input. When OE is high, all outputs are enabled. When OE is low, the outputs are disabled to a high-impedance state. An internal pullup resistor is provided on OE.

Low-power operation also is provided for with $\overline{\text{HCLK\_EN}}$ and $\overline{\text{PCI\_EN}}$ inputs. $\overline{\text{HCLK\_EN}}$, when low, places all host clocks in the logic low state; all other outputs operate normally. $\overline{\text{PCI\_EN}}$, when low, places all PCI clocks in the logic low state; all other outputs operate normally. Internal pulldown resistors are provided on the $\overline{\text{HCLK\_EN}}$ and $\overline{\text{PCI\_EN}}$ inputs.

Because the CDC9163 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power-up and application of a fixed-frequency, fixed-phase signal at the XIN input, as well as following any changes to SEL(0:2).

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TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HCLK(1:12)	47, 45, 42, 41, 39, 38, 37, 36, 34, 33, 9, 8	Output	3.3-V CPU SDRAM Clocks. Twelve HCLKs are programmable with SEL(0:2) as shown in the Frequency-Select table. HCLKs are set low when $\overline{\text{HCLK\_EN}}$ is low.
PCI(1:6)	11, 12, 13, 14, 16, 17	Output	3.3 V PCI Clocks. Six PCI clocks operate at 1/2 the HCLK frequency. PCI clocks are set low when $\overline{\text{PCLK\_EN}}$ is low.
SBCLK	23	Output	Serial bus clock. SBCLK provides 3.3-V universal serial bus 48-MHz clock output.
FCCLK	22	Output	Floppy controller clock. FCCLK provides 3.3-V floppy controller clock output at 24 MHz.
REF(1:2)	1, 2	Output	Reference clock. REF provides 3.3-V ISA reference clock output at 14.318 MHz
XIN	4	Input	Crystal (or oscillator) input
XOUT	5	Output	Crystal output
$\overline{\text{HCLK\_EN}}$	31	Input	Host clock enable. When $\overline{\text{HCLK\_EN}}$ is low, HCLKs are set low. $\overline{\text{HCLK\_EN}}$ has pulldown resistor on the input.
$\overline{\text{PCI\_EN}}$	25	Input	PCI clock enable. When PCI_EN is low, PCIs are low. PCI_EN has a pulldown resistor on the input.
OE	28	Input	Output enable. OE is the output-enable for all outputs except XOUT. When OE is high, outputs are enabled. When OE is low, outputs are disabled to a high-impedence state.
SEL(0:2)	26, 27	Input	Host clock frequency select. SEL operation is shown in frequency-select table.
V_{CC}	20, 21, 28, 48	Power	3.3-V core power supply
$V_{CC(CPU)}$	6, 32, 40, 46	Power	3.3-V host clock output power supply
$V_{CC(PCI)}$	15	Power	3.3-V PCI clock output power supply
GND	3, 10, 18, 19, 24, 30, 35, 43, 44	GND	Ground

FREQUENCY SELECT

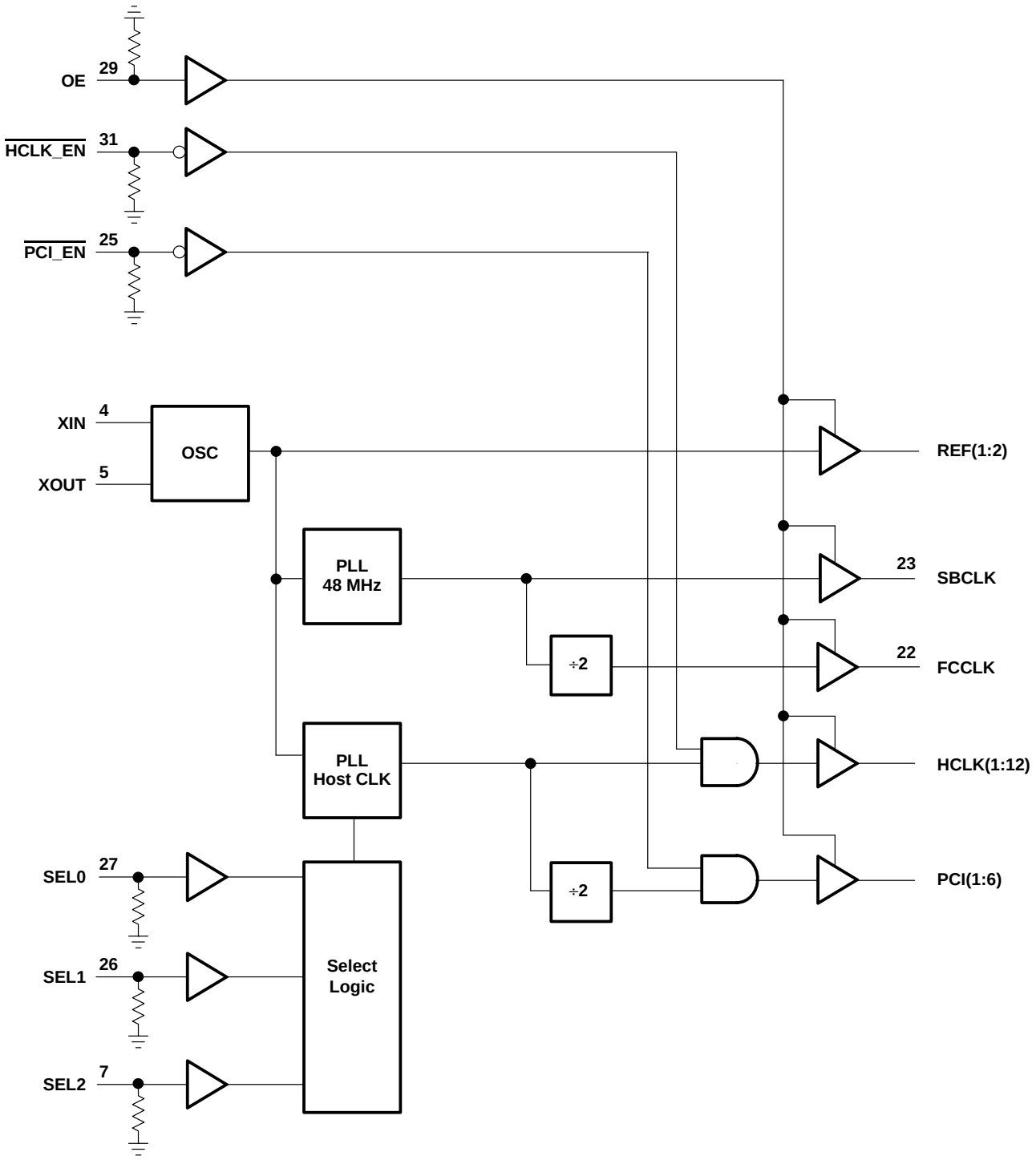
OE	SEL2	SEL1	SEL0	XIN	HCLKn	PCIn	REFn	SBCLK	FCCLK
L	X	X	X	14.31818 MHz†	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	L	L	14.31818 MHz	75 MHz	37.5 MHz	14.318 MHz	48 MHz	24 MHz
H	L	L	H	14.31818 MHz	TBD	TBD	14.318 MHz	48 MHz	24 MHz
H	L	H	L	14.31818 MHz	TBD	TBD	14.318 MHz	48 MHz	24 MHz
H	L	H	H	14.31818 MHz	83.3MHz	41.6 MHz	14.318 MHz	48 MHz	24 MHz
H	H	L	L	14.31818 MHz	50 MHz	25 MHz	14.318 MHz	48 MHz	24 MHz
H	H	L	H	14.31818 MHz	60 MHz	30 MHz	14.318 MHz	48 MHz	24 MHz
H	H	H	L	14.31818 MHz	66.6 MHz	33.3 MHz	14.318 MHz	48 MHz	24 MHz
H	H	H	H	14.31818 MHz	55 MHz	27.5	14.318 MHz	48 MHz	24 MHz

† The allowable reference frequency is minimum = 14.316 MHz, nominal = 14.31818 MHz, and maximum = 14.32 MHz.

CLOCK ENABLE TABLE

$\overline{\text{HCLK\_EN}}$	$\overline{\text{PCI\_EN}}$	HCLKn	PCIn
L	L	Running	Running
L	H	Running	L
H	L	L	Running
H	H	L	L

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
$V_{CC(CPU)}$ . . . . . –0.5 V to 4.6 V
$V_{CC(PCI)}$ . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to V_{CCO} + 0.5 V
Current into any output in the low state, I_O . . . . . 24 max
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	3.3-V core supply voltage	3.135	3.465	V
$V_{CC(CPU)}$	3.3-V I/O supply voltage	3.135	3.465	V
V_{IH}	High-level input voltage	2.0	V_{CCO3}+0.3	V
V_{IL}	Low-level input voltage	–0.3	0.8	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	V_{CC} = 3.135 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CCO3} = 3.135 V,	I_{OH} = –12 mA		2.4		V
V_{OL}	V_{CCO3} = 3.135 V,	I_{OL} = 12 mA			0.4	V
I_I	V_{CC} = 3.465 V,	V_I = V_{CC} or GND		–5	5	µA
I_I, (pullup/pulldown)	V_{CC} = 3.465 V,	V_I = V_{CC} or GND		–100	100	µA
I_{OZ}	V_{CC} = 3.465 V,	V_O = 3.135 V or 0				µA
I_{CC}	V_{CC} = 3.465 V, V_I = V_{CC} or GND	I_O = 0,	Outputs switching			mA
			Outputs low			
			Outputs disabled			
C_i	Except XIN				5	pF
C_o	Except XOUT				6	pF
L_{pin}					7	nH
C_{pd}	V_I = 3.135 V or 0					pF

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
Stabilization time†	After change to SEL0, SEL1, or SEL2		3	ms
	After power up		3	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN.

switching characteristics (see Figures 1, and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
Host clocks					
Jitter†		HCLKn		±250	ps
t_r†‡		HCLKn	0.4	2	ns
t_f†‡		HCLKn	0.4	2	ns
Duty cycle†		HCLKn	45	55	%
t_{skew}†		HCLKn		250	ps
Clock enable latency	$\overline{\text{HCLK\_EN}}$	HCLKn↑	1	4	HCLK cycles
PCI clocks					
Jitter†		PCKLn		±350	ps
t_r†‡		PCKLn	0.5	2.0	ns
t_f†‡		PCKLn	0.5	2.0	ns
Duty cycle†		PCKLn	45	55	%
t_{skew}†		PCKLn		500	ps
$t_{hpoffset}$†	HCLKn	PCKLn	1	4	ns
Clock enable latency	$\overline{\text{PCLK\_EN}}$	PCLKn↑	1	4	HCLK cycles
Fixed clocks (REF, SBCLK, FCCLK)					
t_r†‡		REF1, SBCLK, FCCLK	1	4	ns
		REF0	0.5	2	
t_f†‡		REF1, SBCLK, FCCLK	1	4	ns
		REF0	0.5	2	
Duty cycle†		REF1, SBCLK, FCCLK	45	55	%

† Specifications are applicable only after the PLL stabilization time has elapsed.
‡ Rise and fall times are characterized using the load circuits shown in Figure 1.

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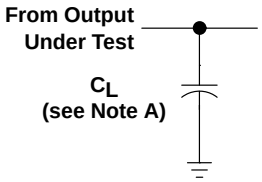
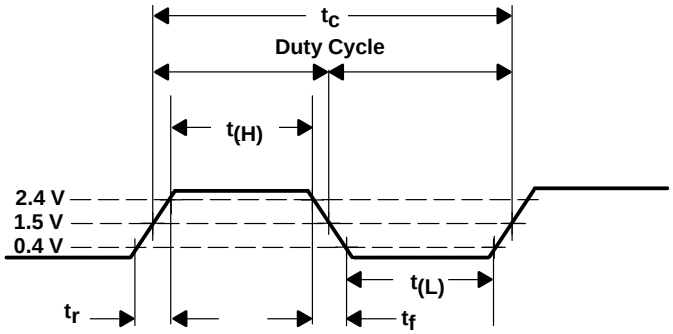
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



3.3-V CLOCK WAVEFORMS

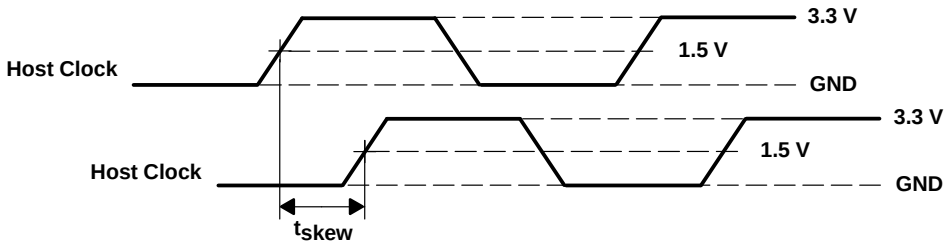
NOTES: A. C_L includes probe and jig capacitance.
- C_L = 20pF (CPUn, REF1, SBCLK, FCCLK)
- C_L = 30pF (PCIn)
- C_L = 45pF (REF0)

B. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

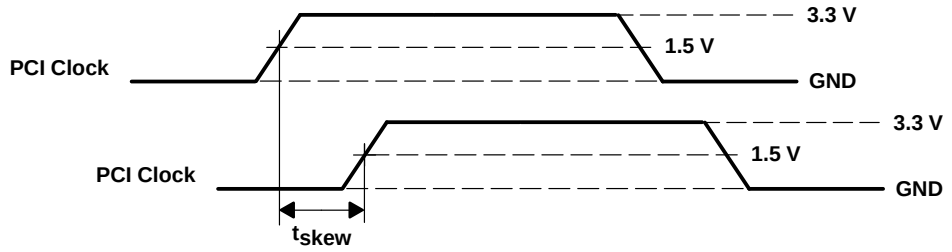
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

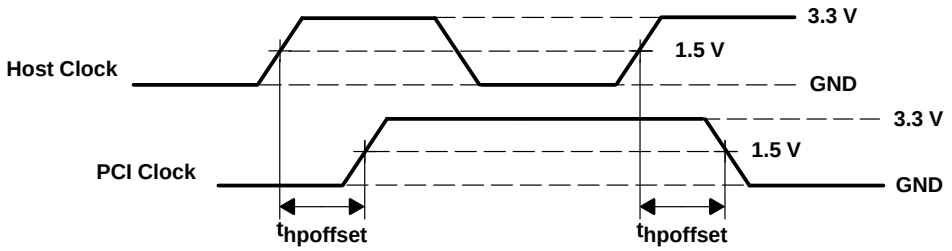
PARAMETER MEASUREMENT INFORMATION



Host-Clock to Host-Clock Skew



PCI-Clock to PCI-Clock Skew



Host-Clock to PCI-Clock Offset

Figure 2. Waveforms for Calculation of $t_{sk(o)}$ and $t_{hpoffset}$

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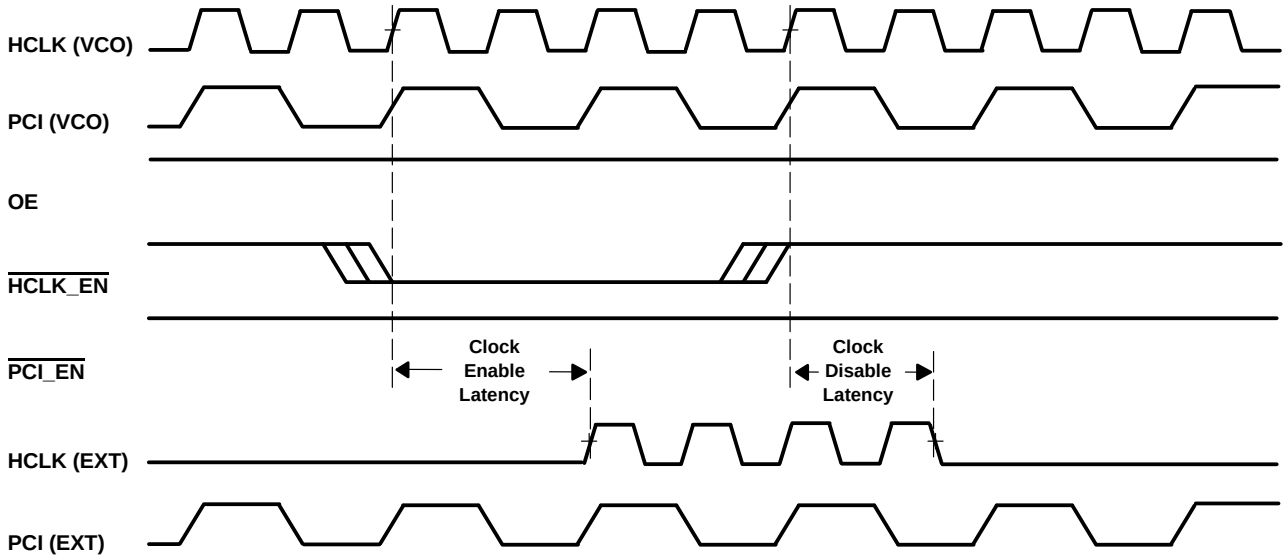
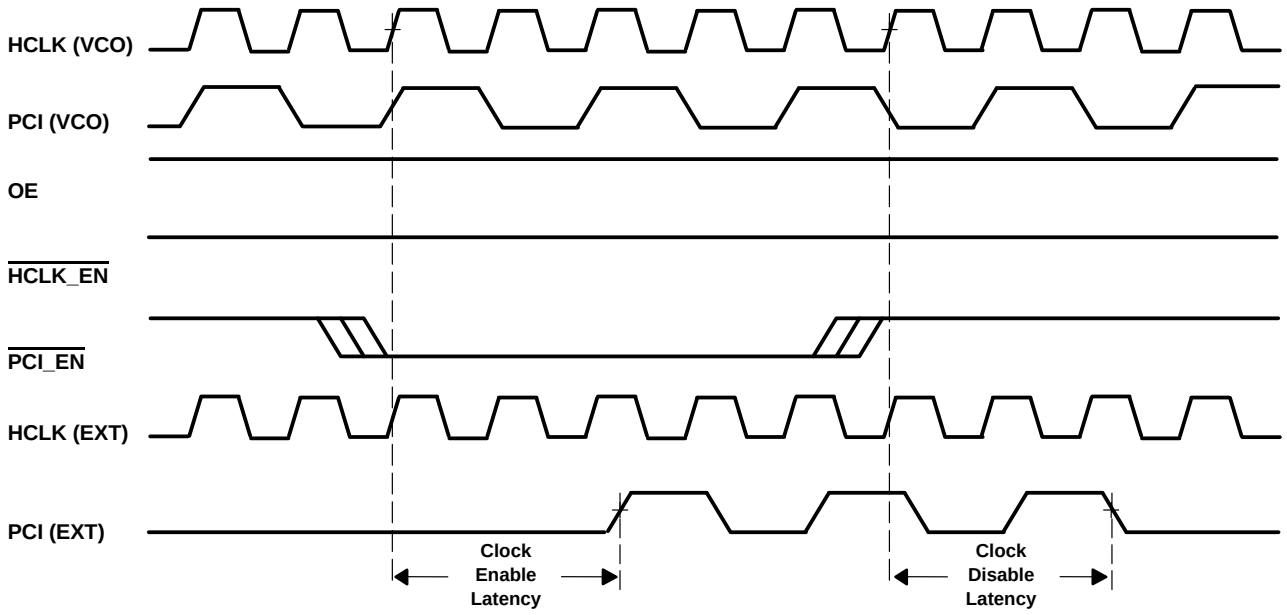
PARAMETER MEASUREMENT INFORMATION



HCLK Enable Timing Diagram



PCLK Enable Timing Diagram

Figure 3. Clock Enable and Disable Latency

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