

# SN74LVCH16240A

## 16-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCAS566D – MARCH 1996 – REVISED MAY 1997

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE  
(TOP VIEW)

$\overline{1OE}$	1	48	$2\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
$V_{CC}$	7	42	$V_{CC}$
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
$V_{CC}$	18	31	$V_{CC}$
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
$4\overline{OE}$	24	25	$3\overline{OE}$

#### description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCH16240A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16240A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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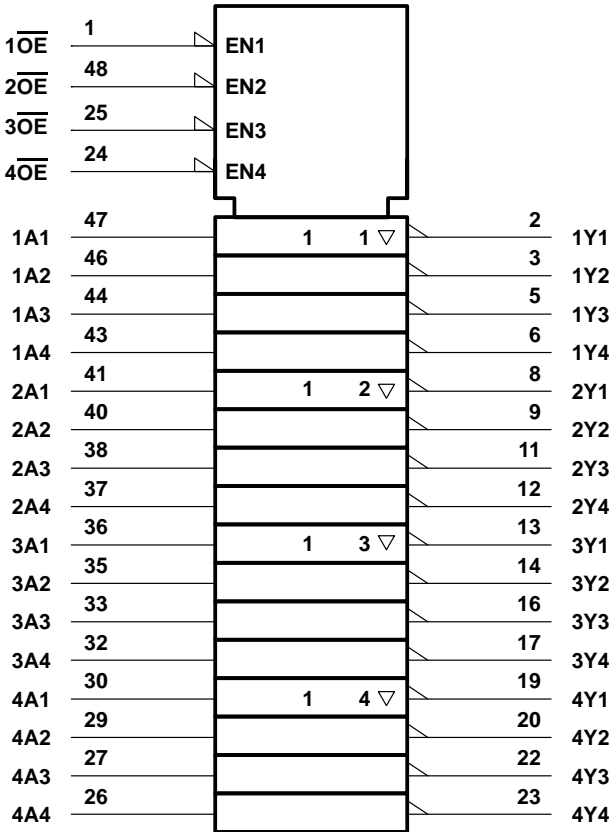
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FUNCTION TABLE  
(each 4-bit buffer)

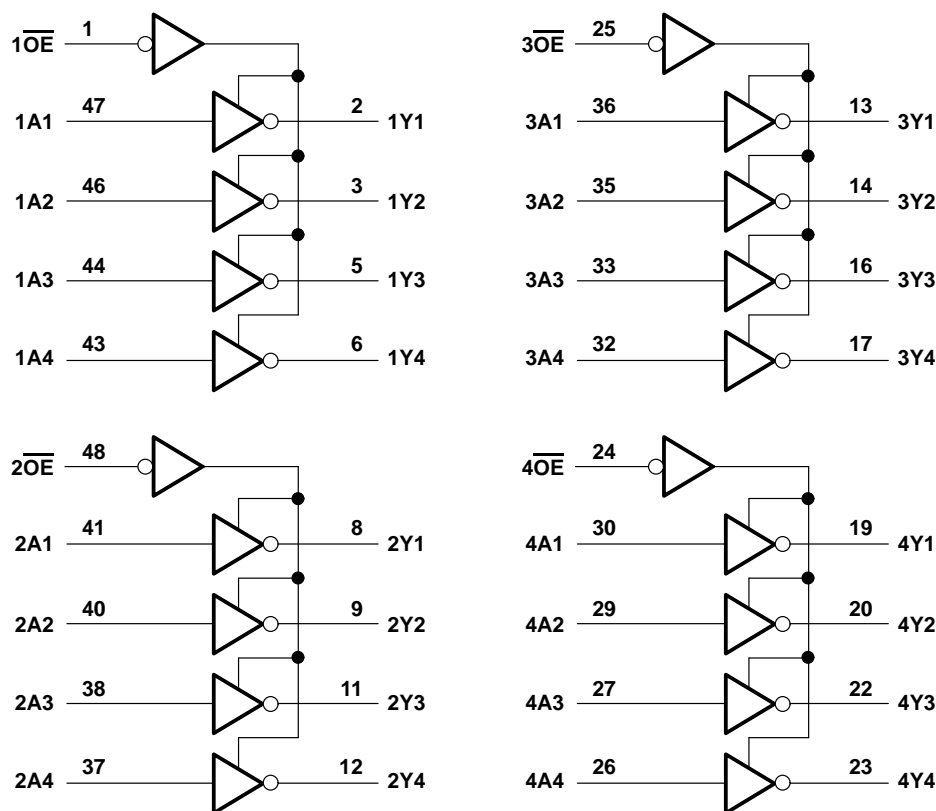
INPUTS		OUTPUT Y
OE	A	
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) (see Note 2)	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
3. The package thermal impedance is calculated in accordance with JESD 51.

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#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3 state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		$V_{CC} = 3 \text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA
		$V_{CC} = 3 \text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
$T_A$	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA		2.7 V to 3.6 V	V <sub>CC</sub> −0.2		V	
	I <sub>OH</sub> = −12 mA		2.7 V	2.2			
			3 V	2.4			
	I <sub>OH</sub> = −24 mA		3 V	2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		2.7 V to 3.6 V	0.2		V	
	I <sub>OL</sub> = 12 mA		2.7 V	0.4			
	I <sub>OL</sub> = 24 mA		3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V		3.6 V	±5		μA	
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.8 V		3 V	75		μA	
	V <sub>I</sub> = 2 V		3 V	−75			
	V <sub>I</sub> = 0 to 3.6 V‡		3.6 V	±500			
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V		2.7 V to 3.6 V	±10		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V	20		μA	
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V§			20			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V,    Other inputs at V <sub>CC</sub> or GND		2.7 V to 3.6 V	500		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V	5		pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	6		pF	

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ This applies in the disabled state only.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	1	4.2	5		ns
$t_{en}$	$\overline{OE}$	Y	1.5	4.7	5.8		ns
$t_{dis}$	$\overline{OE}$	Y	1.5	5.9	6.6		ns
$t_{sk(o)}^\dagger$				1.4			ns

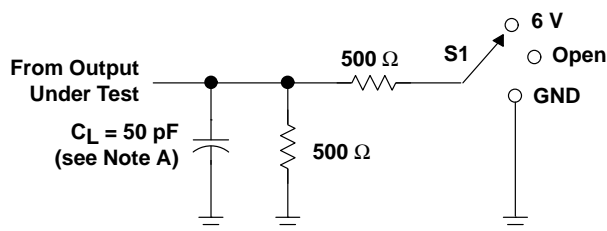
$^\dagger$  Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

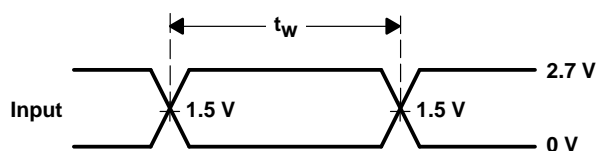
PARAMETER			TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per buffer/driver	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	34	pF
		Outputs disabled		3	



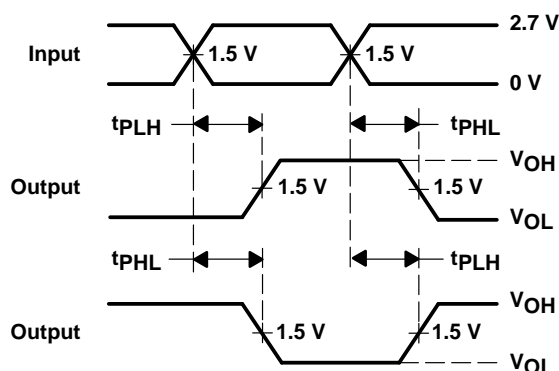
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

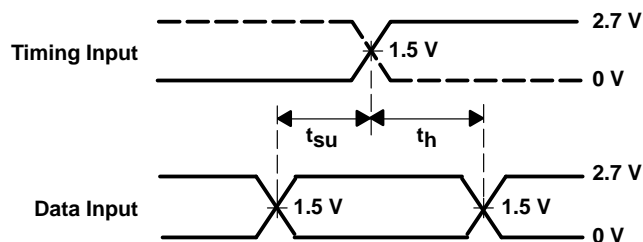


VOLTAGE WAVEFORMS  
PULSE DURATION

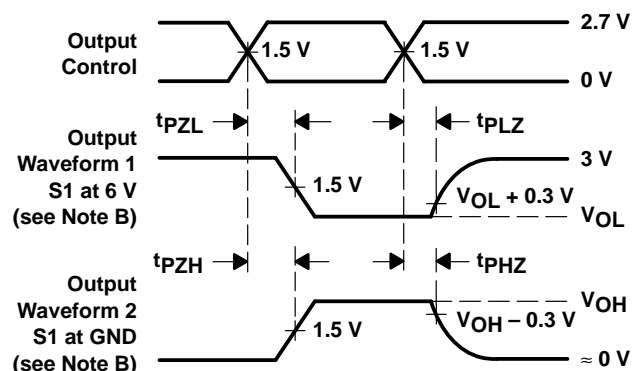


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PHL}$	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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