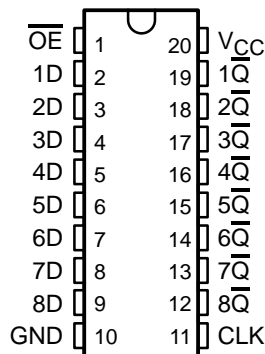


# SN54ACT564, SN74ACT564 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

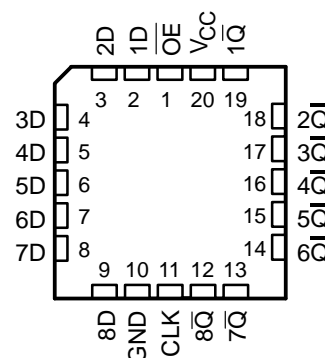
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- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 3-State Inverted Outputs Drive Bus Lines Directly
- Flow-Through Architecture to Optimize PCB Layout
- Full Parallel Access for Loading
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

SN54ACT564 . . . J OR W PACKAGE  
SN74ACT564 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ACT564 . . . FK PACKAGE  
(TOP VIEW)



## description

The 'ACT564 are octal D-type edge-triggered flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the  $\bar{Q}$  outputs are set to the complements of the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ACT564 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ACT564 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\bar{Q}$
L	$\uparrow$	H	L
L	$\uparrow$	L	H
L	H or L	X	$\bar{Q}_0$
H	X	X	Z



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**TEXAS  
INSTRUMENTS**

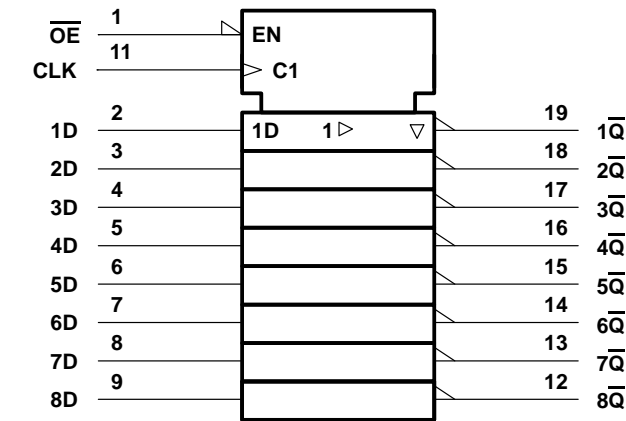
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SN54ACT564, SN74ACT564  
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS  
WITH 3-STATE OUTPUTS

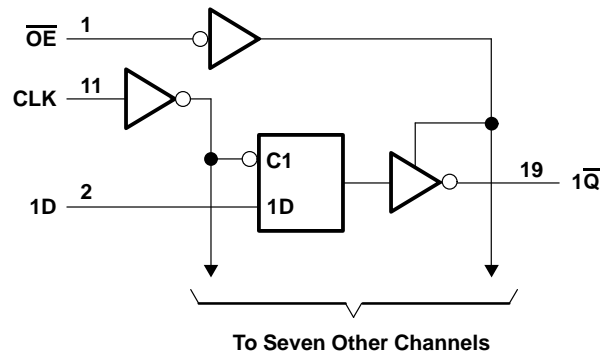
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 200$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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## recommended operating conditions (see Note 3)

		SN54ACT564		SN74ACT564		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-24	mA
$I_{OL}$	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	8	0	8	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54ACT564		SN74ACT564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	$I_{OH} = -24\ \text{mA}$	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	$I_{OH} = -50\ \text{mA}^\dagger$	5.5 V				3.85				
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24\ \text{mA}$	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50\ \text{mA}^\dagger$	5.5 V					1.65			
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 5$		$\pm 2.5$	$\mu\text{A}$
		5.5 V			$\pm 0.1$		$\pm 1$		$\pm 1$	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V		0.6			1.6		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4.5						pF
$C_o$	$V_O = V_{CC}$ or GND	5 V		15						pF

$^\dagger$  Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

$^\ddagger$  This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

## timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\ \text{V} \pm 0.5\ \text{V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54ACT564		SN74ACT564		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, CLK high or low	3		5		3.5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	2.5		3.5		3		ns
$t_h$	Hold time, data after CLK $\uparrow$	1		2.5		1		ns

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# SN54ACT564, SN74ACT564

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54ACT564		SN74ACT564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			85	90		65		75		MHz
$t_{\text{PLH}}$	CLK	$\bar{Q}$	2	6.5	10.5	1	12.5	1.5	11.5	ns
$t_{\text{PHL}}$			1.5	6	9.5	1	11.5	1.5	10.5	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	$\bar{Q}$	1.5	5.5	9	1	10.5	1.5	9.5	ns
$t_{\text{PZL}}$			1.5	5.5	8.5	1	10.5	1	9.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	$\bar{Q}$	1.5	7	10.5	1	12.5	1.5	11.5	ns
$t_{\text{PLZ}}$			1.5	5	8	1	9.5	1	8.5	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	50	pF

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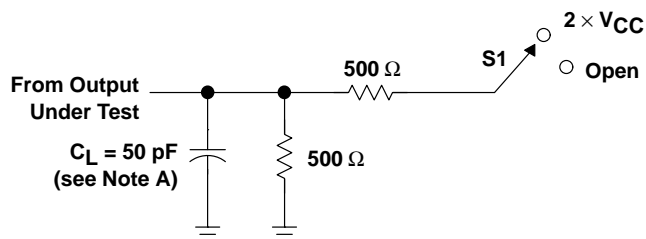


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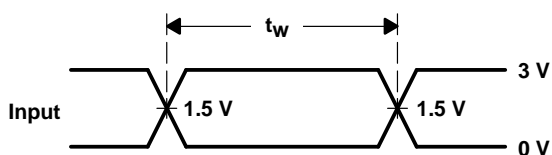
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## PARAMETER MEASUREMENT INFORMATION

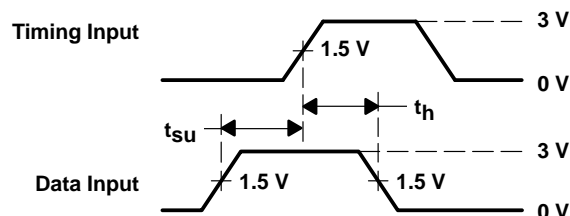


LOAD CIRCUIT

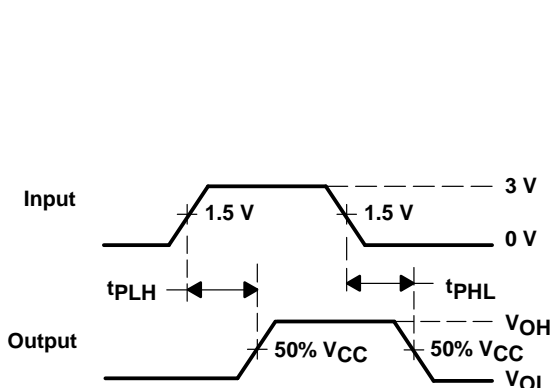
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



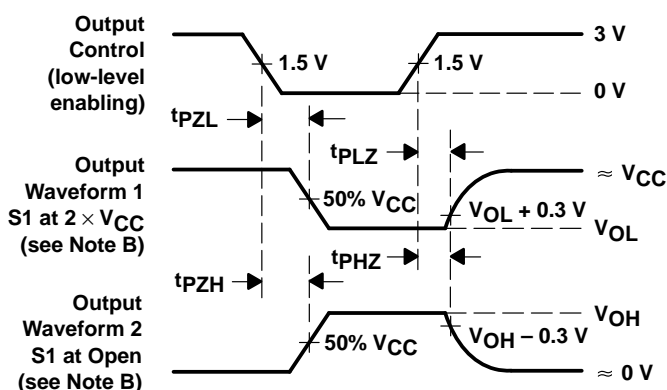
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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