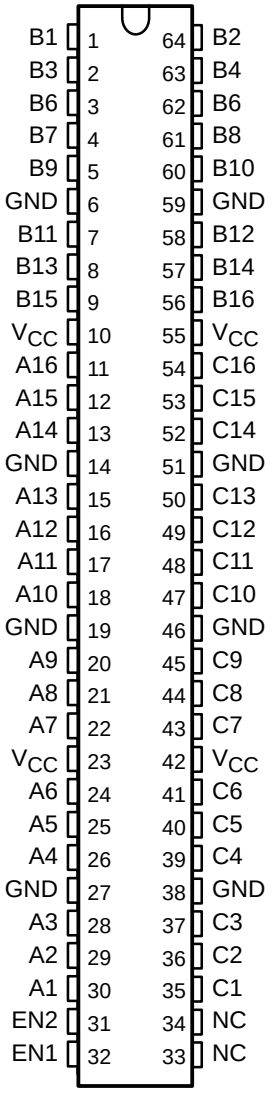
- **Member of the Texas Instruments *Widebus*™ Family**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Packaged in Plastic Thin Shrink Small-Outline (DGG) Package**

DGG PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 74ACT16254 is a dual 16-bit, noninverting bus-interface device. The A and C ports perform a transceiver function, like that of the 74ACT245. The B and C ports perform the buffer/driver function of the 74ACT244. The A and C port outputs are designed to sink up to 12 mA.

The 74ACT16254 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

Data transmission from the A port to the C port, C port to A port, or B port to C port is accomplished by setting the appropriate logic levels on the bus enable (EN1 and EN2) inputs.

All outputs are disabled when logic highs are placed on both EN1 and EN2; the buses are effectively isolated.

The 74ACT16254 is packaged in TI's thin shrink small-outline package (DGG), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Active bus-hold circuitry is provided to hold unused or floating data and I/O pins at a valid logic level.

The 74ACT16254 is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

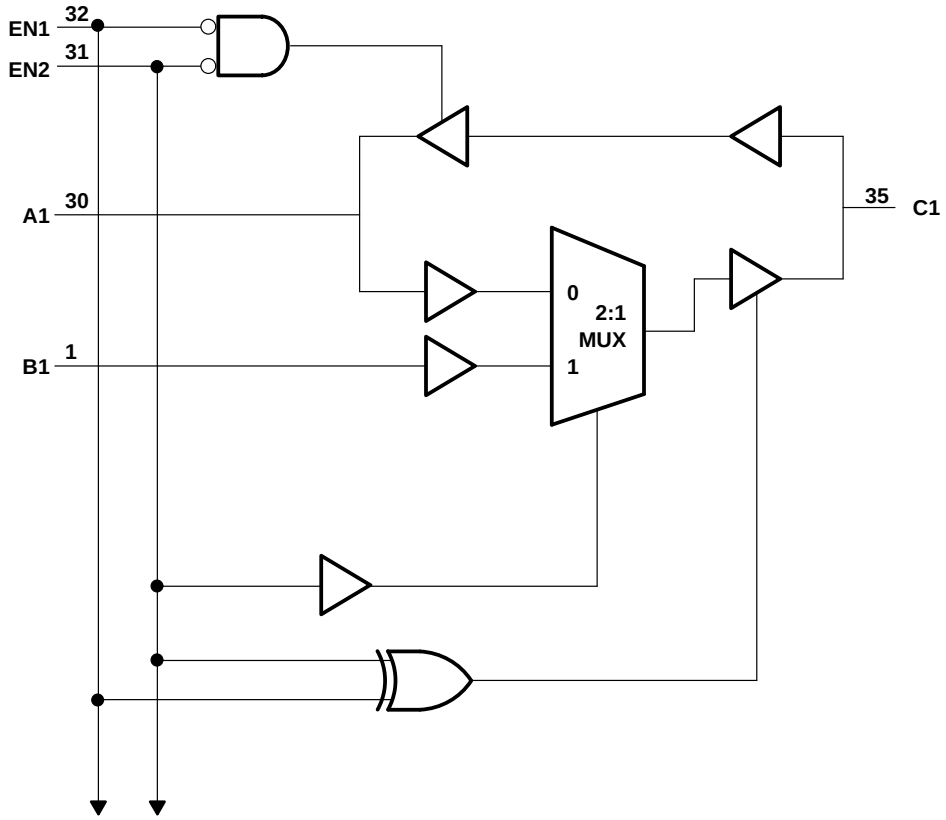
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1995, Texas Instruments Incorporated

FUNCTION TABLE

INPUTS		OPERATION
EN2	EN1	
H	H	Isolation
H	L	B data to C bus
L	H	A data to C bus
L	L	C data to A bus

logic diagram, each port (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 50 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –100 μA		3			V
	V_{CC} = 5.5 V,	I_{OH} = –100 μA		4.2			
	V_{CC} = 4.5 V,	I_{OH} = –12 mA		3			
V_{OL}	V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 100 μA				0.1	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA				0.4	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND	Inputs only			±10	μA
I_{hold}	V_{CC}= 4.5 V,	V_I = 2 V	A, B, or C port	–100			μA
	V_{CC} = 4.5 V,	V_I = 0.8 V		100			
I_{OZ}‡	V_{CC} = 5.5 V,	V_O = V_{CC} or GND				±20	μA
I_{CC}	V_{CC} = 5.5 V, I_O = 0,	V_I = V_{CC} or GND				50	μA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				500	μA
C_i	V_{CC} = 5 V,	V_I = V_{CC} or GND			3.5		pF
C_{io}	V_{CC} = 5 V,	V_O = V_{CC} or GND			5		pF

† All typical values are at T_A = 25°C.
‡ The parameter I_{OZ} includes the input-leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

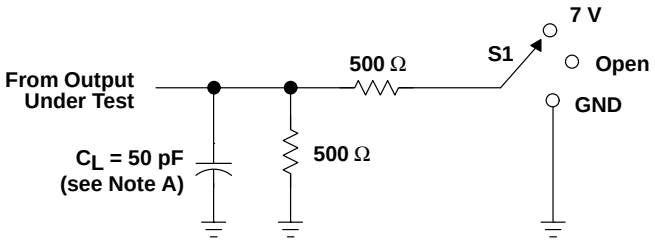
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UNIT
			MIN	TYP	MAX	
t_{pd}	A or B	C	1.5	3.7	6.2	ns
t_{pd}	C	A	1.5	3.3	5.5	ns
t_{en}	EN1 or EN2	C	1.5	5.3	9.5	ns
t_{dis}	EN1 or EN2	C	1.5	4.4	8	ns
t_{en}	EN2	A	1.5	6.2	10.5	ns
t_{dis}	EN2	A	1.5	4.8	8	ns

operating characteristics, T_A = 25°C

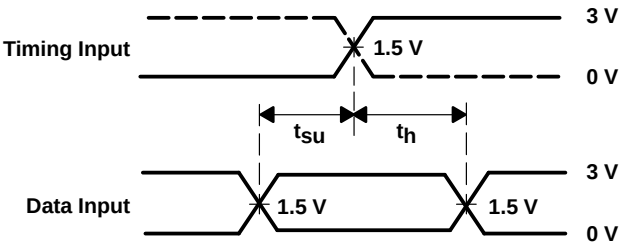
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	16	pF
		Outputs disabled		2	pF

PARAMETER MEASUREMENT INFORMATION

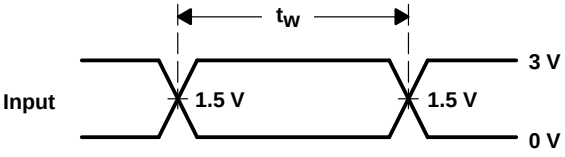


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

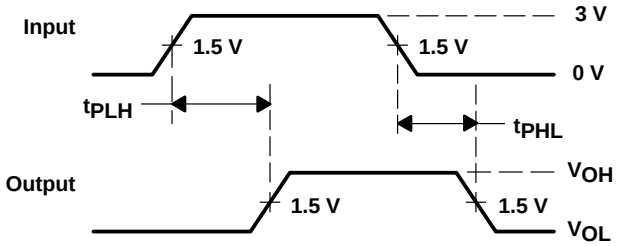
LOAD CIRCUIT



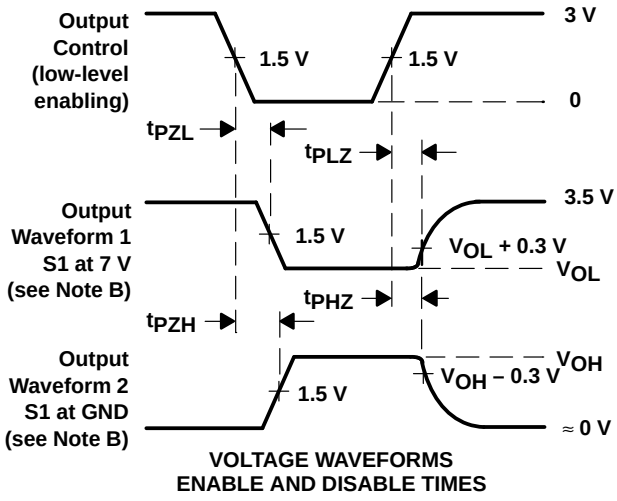
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated