

SN54AC74, SN74AC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

SCAS521C – AUGUST 1995 – REVISED SEPTEMBER 1996

- **EPIC™** (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Flat (W), and DIP (J,N) Packages

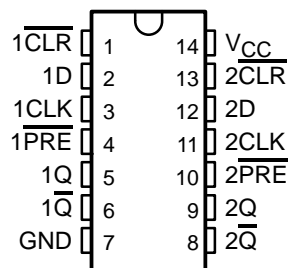
description

The 'AC74 are dual positive-edge-triggered D-type flip-flops.

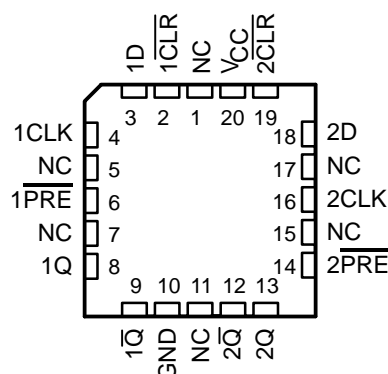
A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

The SN54AC74 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AC74 is characterized for operation from -40°C to 85°C .

SN54AC74 ... J OR W PACKAGE
SN74AC74 ... D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AC74 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{\text{Q}}_0$

† This configuration is unstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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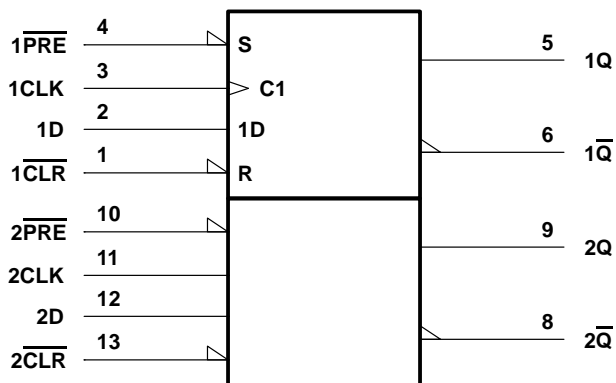
SN54AC74, SN74AC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

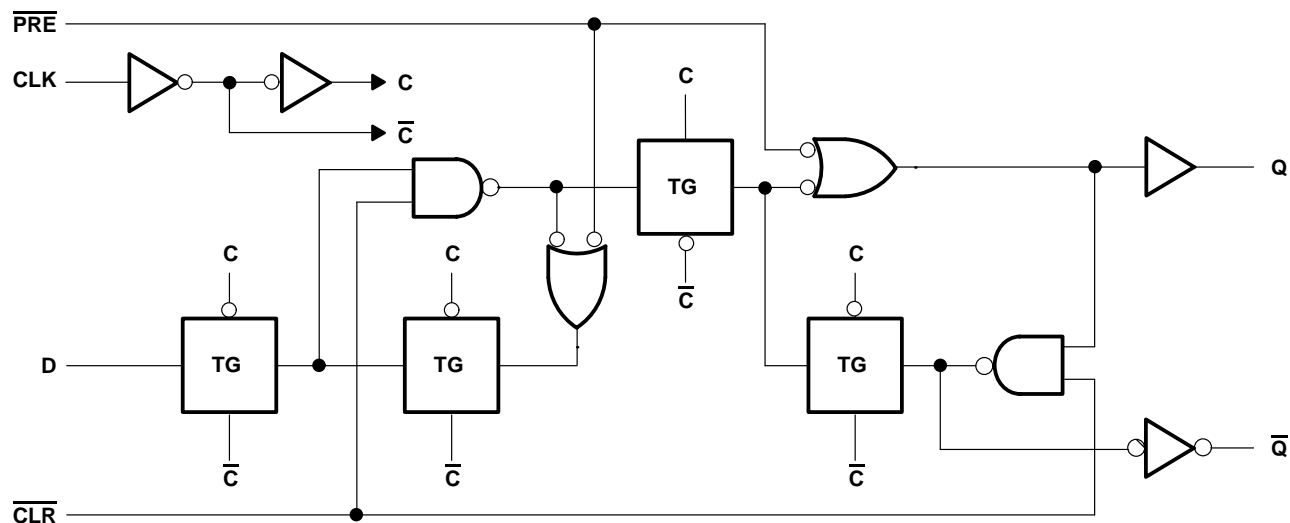
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram, each flip-flop (positive logic)



SN54AC74, SN74AC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

SCAS521C – AUGUST 1995 – REVISED SEPTEMBER 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB package	0.5 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1		2.1		V
		$V_{CC} = 4.5$ V	3.15		3.15		
		$V_{CC} = 5.5$ V	3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9		0.9	V
		$V_{CC} = 4.5$ V		1.35		1.35	
		$V_{CC} = 5.5$ V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V		–12		–12	mA
		$V_{CC} = 4.5$ V		–24		–24	
		$V_{CC} = 5.5$ V		–24		–24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12		12	mA
		$V_{CC} = 4.5$ V		24		24	
		$V_{CC} = 5.5$ V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	8	0	8	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



SN54AC74, SN74AC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLEAR AND PRESET

SCAS521C – AUGUST 1995 – REVISED SEPTEMBER 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AC74		SN74AC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9	4.49		2.9		2.9		V	
		4.5 V	4.4	5.49		4.4		4.4			
		5.5 V	5.4	5.49		5.4		5.4			
	I _{OH} = -12 mA	3 V	2.56			2.4		2.46			
	I _{OH} = -24 mA	4.5 V	3.86			3.7		3.76			
		5.5 V	4.86			4.7		4.76			
	I _{OH} = -50 mA†	5.5 V				3.85					
I _{OH} = -75 mA†	5.5 V						3.85				
V _{OL}	I _{OL} = 50 μA	3 V		0.002	0.1		0.1		0.1	V	
		4.5 V		0.001	0.1		0.1		0.1		
		5.5 V		0.001	0.1		0.1		0.1		
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44		
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44		
		5.5 V			0.36		0.5		0.44		
	I _{OL} = 50 mA†	5.5 V				1.65					
	I _{OL} = 75 mA†	5.5 V						1.65			
I _I	Data pins	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1	μA	
	Control pins				±0.1		±1		±1		
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			2		40		20	μA
C _i		V _I = V _{CC} or GND	5 V		3						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

			T _A = 25°C		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	100	0	100	0	100	MHz
t _w	Pulse duration	PRE or CLR low	5.5		8		7		ns
		CLK	5.5		8		7		
t _{su}	Setup time, data before CLK↑	Data	4		5		4.5		ns
		PRE or CLR inactive	0		0.5		0		
t _h	Hold time, data after CLK↑		0.5		0.5		0.5		ns



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SN54AC74, SN74AC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SCAS521C – AUGUST 1995 – REVISED SEPTEMBER 1996

**timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

			$T_A = 25^\circ\text{C}$		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	140	0	140	0	140	MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4.5		5.5		5		ns
		CLK	4.5		5.5		5		
t_{su}	Setup time, data before CLK \uparrow	Data	3		4		3		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0		0.5		0		
t_h	Hold time, data after CLK \uparrow		0.5		0.5		0.5		ns

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		70		95		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3.5	8	12	1	13	2.5	13	ns
t_{PHL}			4	10.5	12	1	14	3.5	13.5	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	4.5	8	13.5	1	17.5	4	16	ns
t_{PHL}			3.5	8	14	1	13.5	3.5	14.5	

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			140	160		95		125		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	2.5	6	9	1	9.5	2	10	ns
t_{PHL}			3	8	9.5	1	10.5	2.5	10.5	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	3.5	6	10	1	12	3	10.5	ns
t_{PHL}			2.5	6	10	1	10	2.5	10.5	

operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

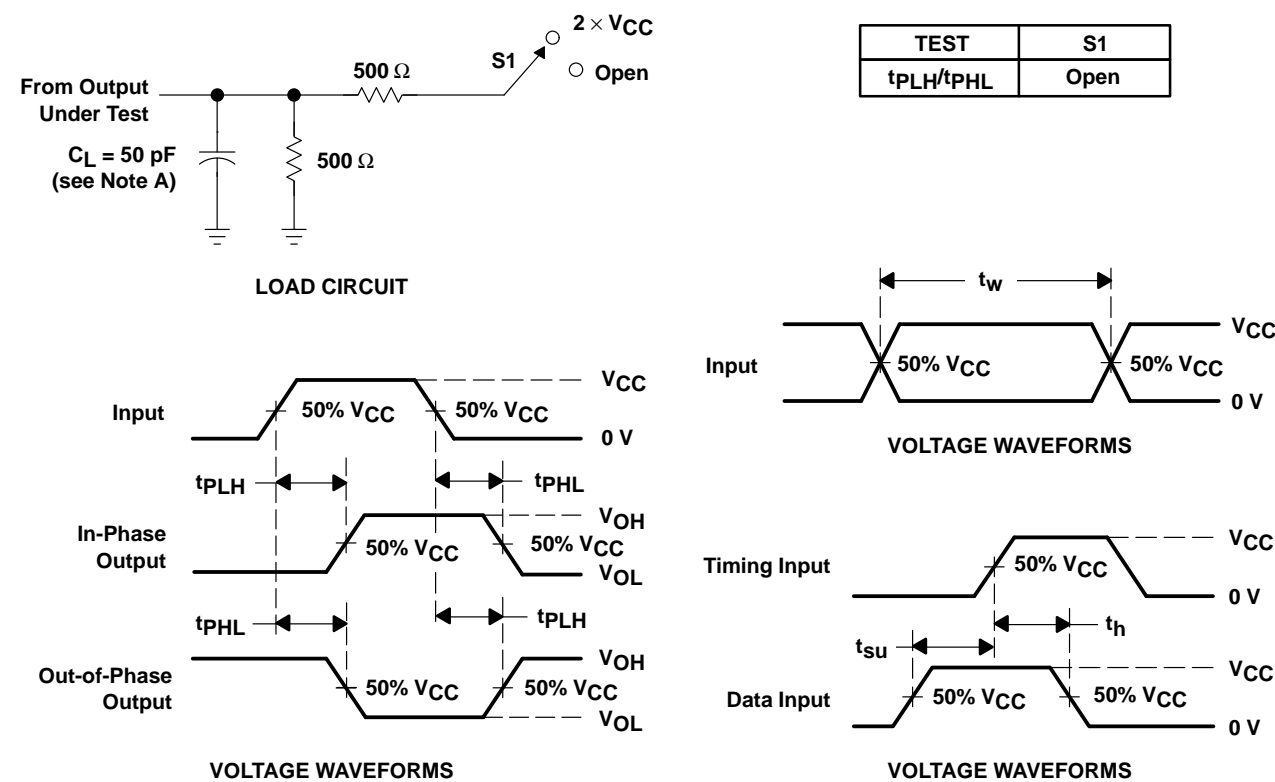
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 1\text{ MHz}$	45	pF



SN54AC74, SN74AC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SCAS521C – AUGUST 1995 – REVISED SEPTEMBER 1996

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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