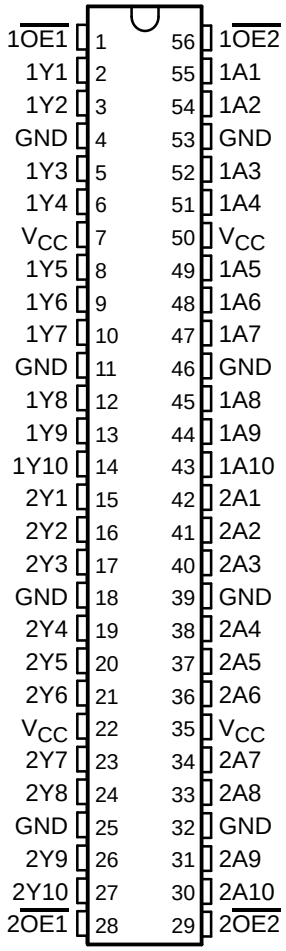
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHP} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Bus Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit noninverting buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation; it is tested at 2.5-V, 2.7-V, and 3.3-V V_{CC}.

The SN74ALVC162827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The SN74ALVC162827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

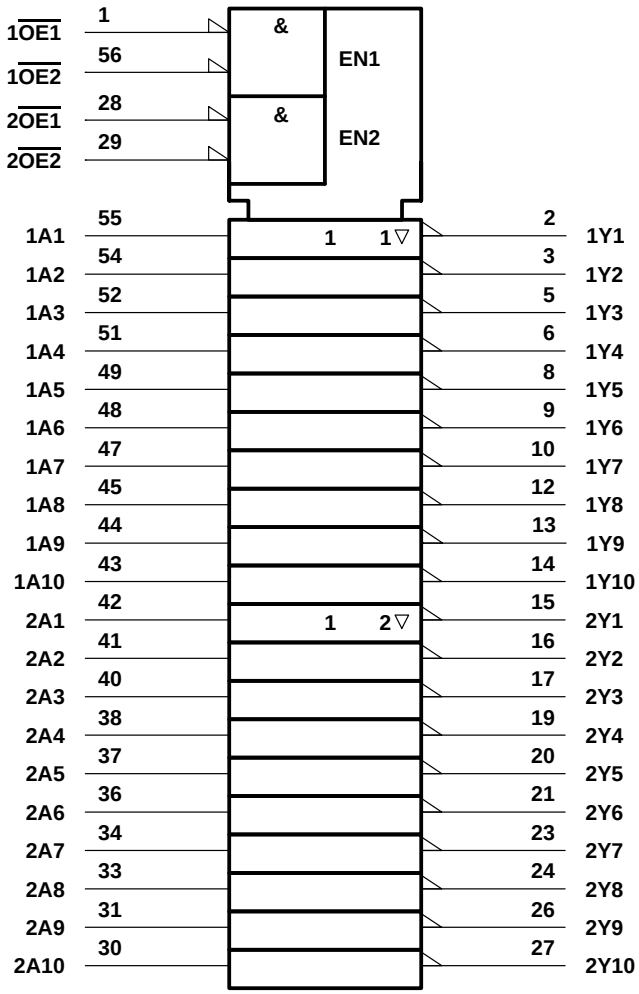
The SN74ALVC162827 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

FUNCTION TABLE
(each 8-bit section)

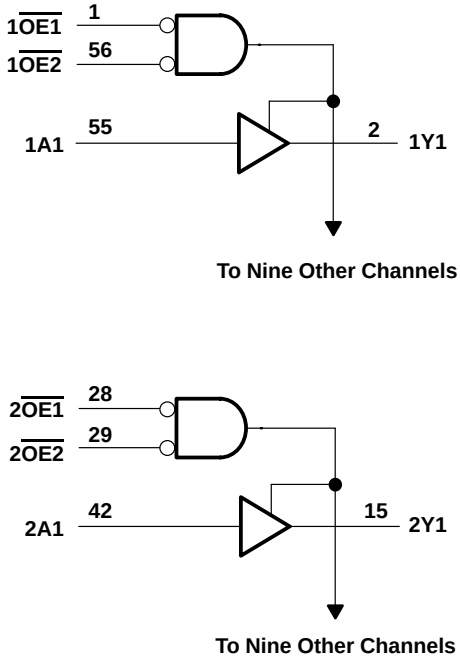
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V			mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V			mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = –4 mA	V_{IH} = 1.7 V	2.3 V				
		V_{IH} = 2 V	2.7 V	2.4			
	I_{OH} = –6 mA,	V_{IH} = 2 V	3 V	2.4			
	I_{OH} = –8 mA	V_{IH} = 1.7 V	2.3 V				
		V_{IH} = 2 V	2.7 V				
	I_{OH} = –12 mA,	V_{IH} = 2 V	3 V				
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 4 mA	V_{IL} = 0.7 V	2.3 V				
		V_{IL} = 0.8 V	2.7 V			0.4	
	I_{OL} = 6 mA,	V_{IL} = 0.8 V	3 V			0.55	
	I_{OL} = 8 mA	V_{IL} = 0.7 V	2.3 V				
		V_{IL} = 0.8 V	2.7 V				
	I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$	V_I = 0.7 V		2.3 V	45			µA
	V_I = 1.7 V			–45			
	V_I = 0.8 V		3 V	75			
	V_I = 2 V			–75			
I_{OZ}‡	V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				750	µA
C_i	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_o	V_O = V_{CC} or GND		3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the paramter I_{OZ} includes the input-leakage current.

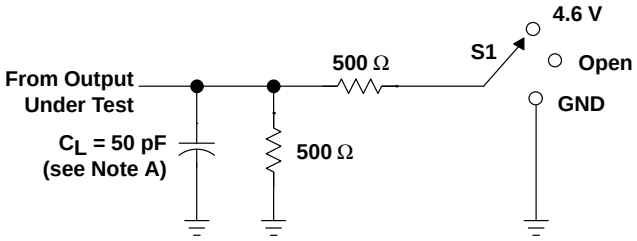
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}									ns
t_{en}									ns
t_{dis}									ns

operating characteristics, T_A = 25°C

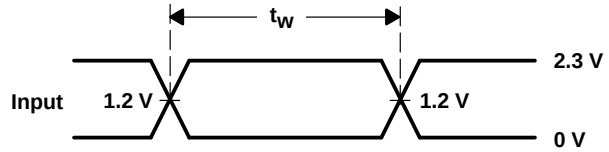
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz			pF
		Outputs disabled				

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

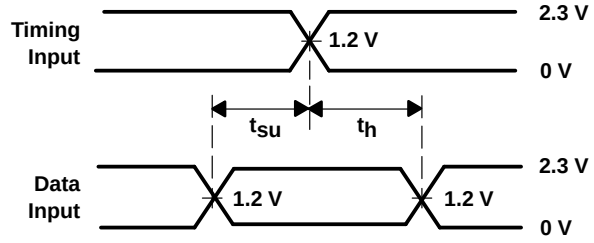


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

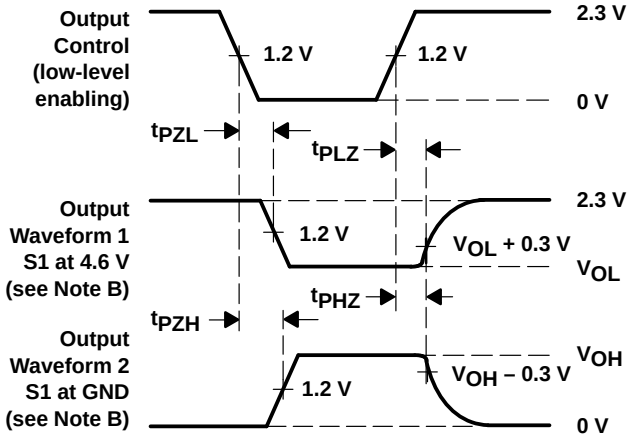
LOAD CIRCUIT



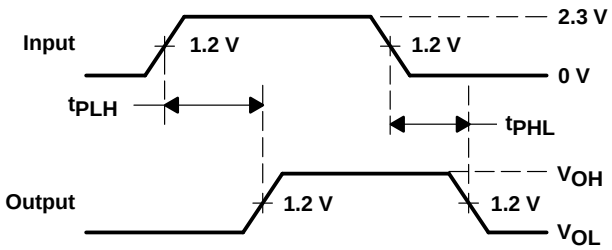
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



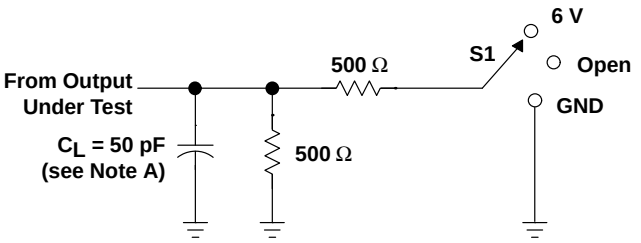
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

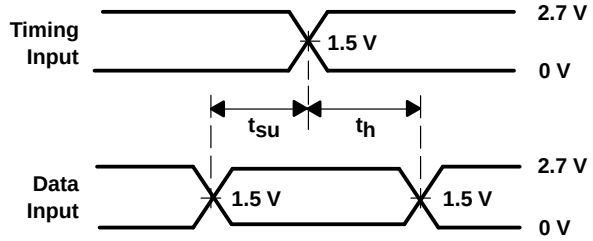
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

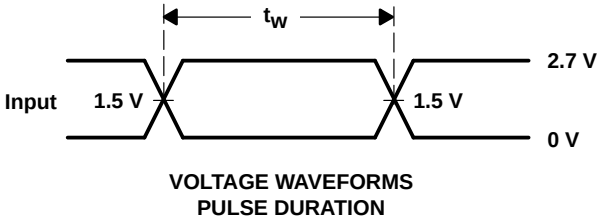


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

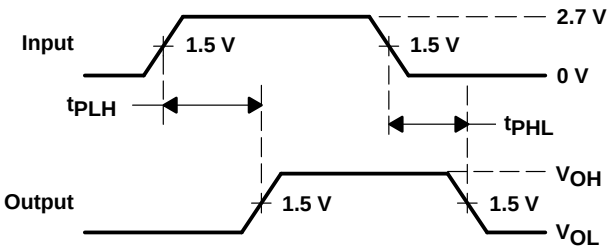
LOAD CIRCUIT



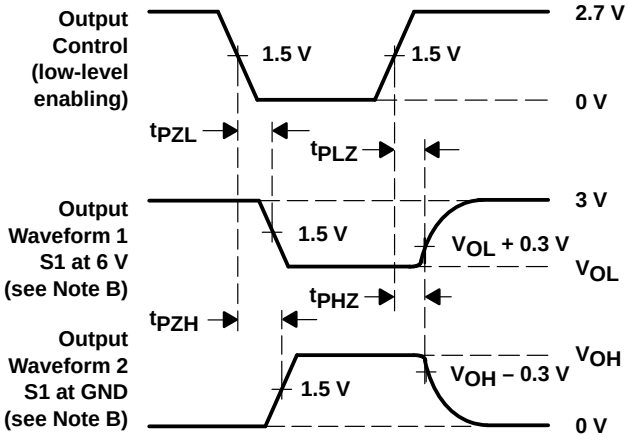
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
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D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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