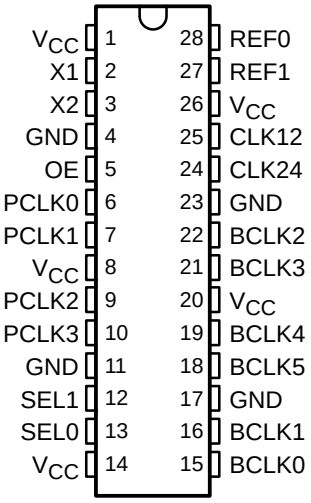
- **Four CPU Clock Outputs With Programmable Frequency (50 MHz, 60 MHz, and 66 MHz)**
- **Six Clock Outputs at Half-CPU Frequency for PCI**
- **One 24-MHz Clock Output**
- **One 12-MHz Clock Output**
- **Two 14.318-MHz Reference Outputs**
- **All Output Clock Frequencies Derived From a Single 14.31818-MHz Crystal Input**
- **LVTTL-Compatible Inputs and Outputs**
- **Internal Loop Filters for Phase-Lock Loops Eliminate the Need for External Components**
- **Operates at 3.3 V_{CC}**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)



description

The CDC9841 is a high-performance clock synthesizer/driver that generates all required clock signals necessary for a high-performance PC motherboard. The four central processing unit (CPU) clock outputs (PCLKn) are programmable to one of three frequencies (50 MHz, 60 MHz, or 66 MHz) via the SEL0 and SEL1 control inputs. The six peripheral-component-interconnect (PCI) clock outputs (BCLKn) are half the frequency of PCLKn and are delayed 1 ns to 4 ns from the rising edge of the CPU clock. In addition, the four fixed-frequency outputs provide a 24-MHz clock (CLK24), a 12-MHz clock (CLK12), and two buffered copies of the 14.318-MHz input reference (REF0, REF1).

The CDC9841 generates all output frequencies from a 14.31818-MHz crystal input. A reference clock can be provided at X1 instead of a crystal input.

Two phase-lock loops (PLLs) generate the CPU clock frequency and the 24-MHz clock frequency. On-chip loop filters and internal feedback eliminate the need for external components. The PCI and 12-MHz clock frequencies are derived from the base CPU and 24-MHz clock frequencies, respectively. The PLL circuit can be bypassed in the TEST mode (i.e., SEL0 = SEL1 = H) to distribute a test clock provided at the X1 input. Because the CDC9841 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at the X1 input, as well as following any changes to the SELn inputs.

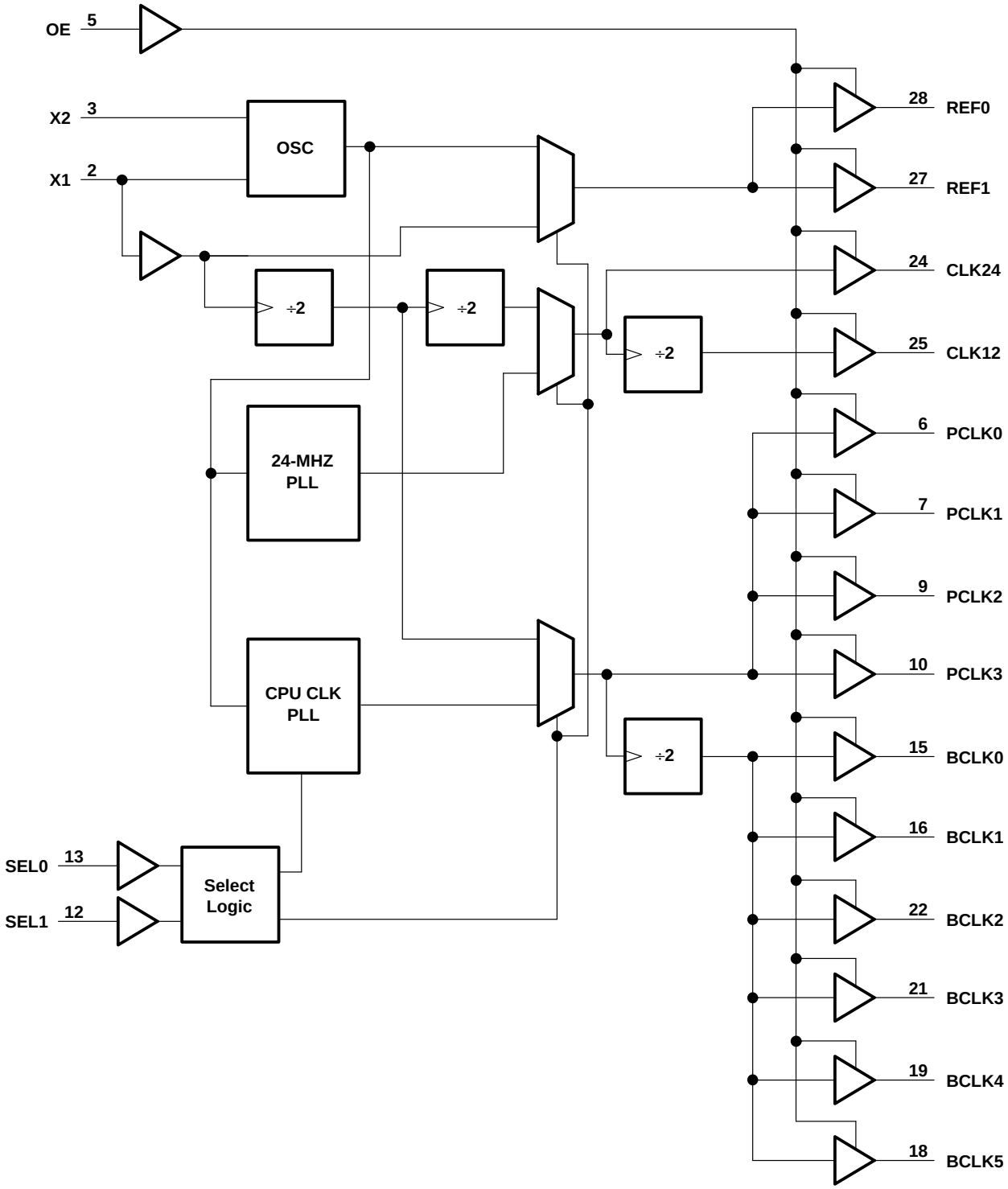
PCLKn and BCLKn provide low-skew/low-jitter clock signals for reliable clock operation. All outputs are 3 state and are enabled via OE.

FUNCTION TABLE

OE	SEL0	SEL1	X1	PCLKn	BCLKn	REFn	CLK24	CLK12
L	X	X	14.31818 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	L	14.31818 MHz	50 MHz	25 MHz	14.318 MHz	24 MHz	12 MHz
H	L	H	14.31818 MHz	60 MHz	30 MHz	14.318 MHz	24 MHz	12 MHz
H	H	L	14.31818 MHz	66 MHz	33 MHz	14.318 MHz	24 MHz	12 MHz
H	H	H	TCLK†	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

† TCLK is a test clock input at the X1 input during test mode.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state,
V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 2 × I_{OHmax}
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.135	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current	REF0		–12	mA
		REF1		–8	
		PCLKn		–6	
		BCLKn		–12	
		CLK24, CLK12		–4	
I_{OL}	Low-level output current	REF0		12	mA
		REF1		8	
		PCLKn		6	
		BCLKn		12	
		CLK24, CLK12		4	
T_A	Operating free-air temperature		0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	V_{CC} = 3.135 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 3.135 V	I_{OH} = –12 mA	REF0	2.5		V
		I_{OH} = –8 mA	REF1	2.5		
		I_{OH} = –6 mA	PCLKn	2.5		
		I_{OH} = –12 mA	BCLKn	2.5		
		I_{OH} = –4 mA	CLK24, CLK12	2.5		
V_{OL}	V_{CC} = 3.135 V	I_{OL} = 12 mA	REF0		0.4	V
		I_{OL} = 8 mA	REF1		0.4	
		I_{OL} = 6 mA	PCLKn		0.4	
		I_{OL} = 12 mA	BCLKn		0.4	
		I_{OL} = 4 mA	CLK24, CLK12		0.4	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	µA
I_{OZ}	V_{CC} = 3.6 V,	V_O = V_{CC} or GND			±10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs enabled†		50	mA
			Outputs disabled		1	
C_i	V_I = V_{CC} or GND					pF
C_o	V_O = V_{CC} or GND					pF
C_{pd}	V_I = 3 V or 0					pF

† Device in normal operating mode with no load on outputs

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
Stabilization time‡	After SEL1, SEL0		5	ms
	After OE↑		5	
	After power up		5	

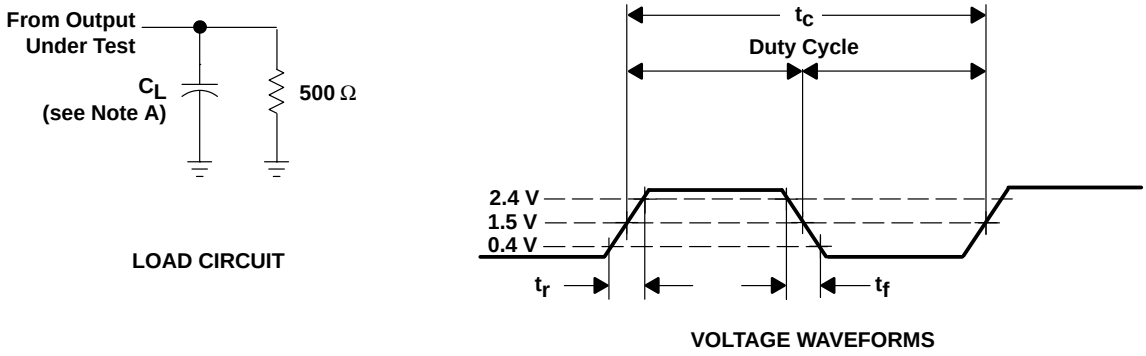
‡ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at X1. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

switching characteristics (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 3.135 V to 3.6 V, T_A = 0°C to 70°C		UNIT
				MIN	MAX	
t_{skew}†		PCLKn (C_L = 20 pF)			200	ps
		BCLKn (C_L = 30 pF)			400	
Offset†	PCLKn (C_L = 20 pF)	BCLKn (C_L = 30 pF)		1	4	ns
Jitter‡		PCLKn (C_L = 20 pF)			±250	ps
		BCLKn (C_L = 30 pF)			±350	
Duty cycle†		Any output		45%	55%	
t_c		PCLKn (C_L = 20 pF)	SEL0 = L, SEL1 = L	20		ns
			SEL0 = L, SEL1 = H	16.7		
			SEL0 = H, SEL1 = L	15		
		BCLKn (C_L = 30 pF)	SEL0 = L, SEL1 = L	40		
			SEL0 = L, SEL1 = H	33.3		
			SEL0 = H, SEL1 = L	30		
t_r†‡		PCLKn (C_L = 20 pF), BCLKn (C_L = 30 pF)			2	ns
t_f†‡		PCLKn (C_L = 20 pF), BCLKn (C_L = 30 pF)			2	ns

† Specifications are applicable only after the PLL stabilization time has elapsed.
‡ Rise and fall times are characterized using the load circuits shown in Figure 1.

PARAMETER MEASUREMENT INFORMATION
CLOCK DRIVER CIRCUITS



NOTES: A. C_L includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

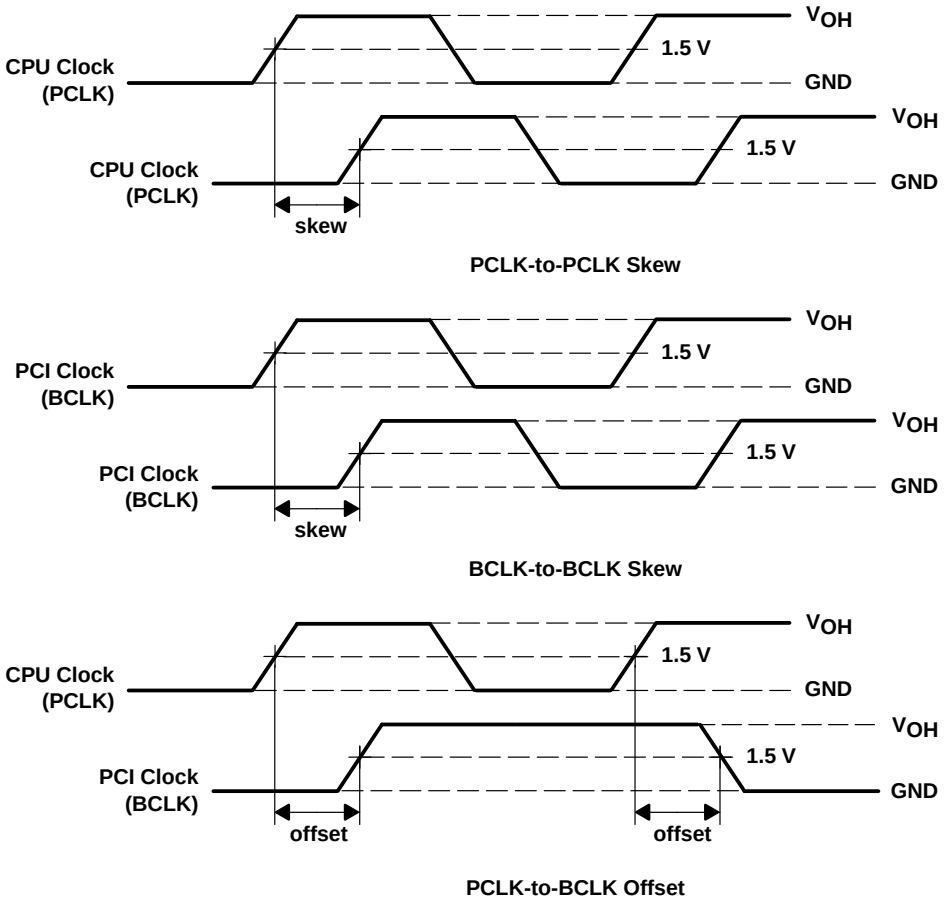


Figure 2. Waveforms for Calculation of t_{skew} and Offset

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