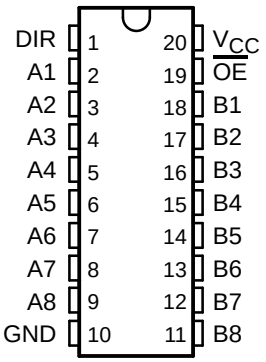
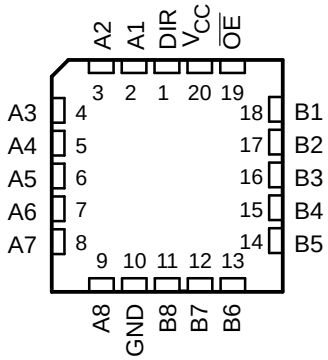
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and DIP (N), Ceramic Chip Carriers (FK), Flat (W), and DIP (J) Packages**

**SN54ACT245 . . . J OR W PACKAGE**
**SN74ACT245 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54ACT245 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

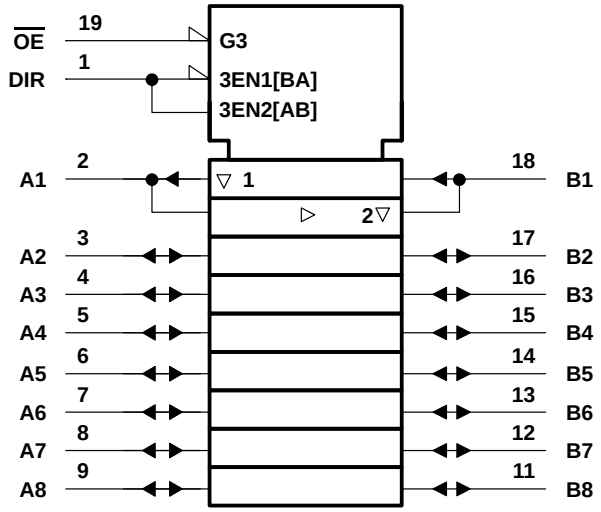
When the output-enable ($\overline{OE}$) is low, the device passes noninverted data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. A high on $\overline{OE}$ disables the device so that the buses are effectively isolated.

The SN54ACT245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT245 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

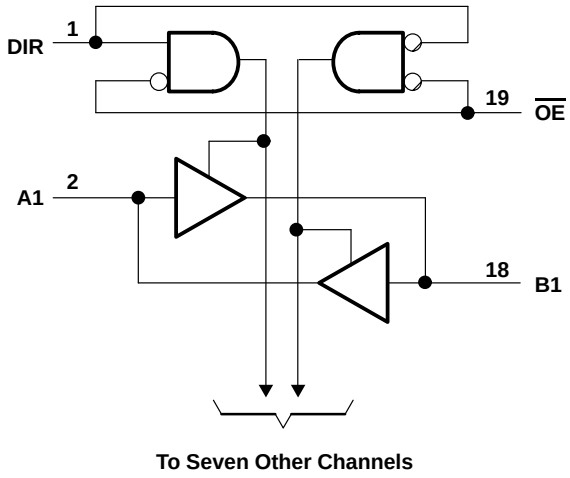
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

### logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±200 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DB package . . . . . 0.6 W
DW package . . . . . 1.6 W
PW package . . . . . 0.7 W
N package . . . . . 1.3 W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54ACT245 | | SN74ACT245 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 8 | 0 | 8 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54ACT245 | | SN74ACT245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = – 50 μA | 4.5 V | 4.4 | 4.49 | | 4.4 | | 4.4 | | V |
| | | | 5.5 V | 5.4 | 5.49 | | 5.4 | | 5.4 | | |
| | | $I_{OH}$ = – 24 mA | 4.5 V | 3.88 | | | 3.7 | | 3.76 | | |
| | | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| | | $I_{OH}$ = –50 mA† | 5.5 V | | | | 3.85 | | | | |
| | | $I_{OH}$ = –75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 5.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_{OZ}$ | A or B ports‡ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.5 | | ±10 | | ±5 | μA |
| $I_I$ | $\overline{OE}$ or DIR | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 80 | | 40 | μA |
| $\Delta I_{CC}$§ | | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | | 0.6 | | 1.6 | | 1.5 | mA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |
| $C_{io}$ | | $V_O = V_{CC}$ or GND | 5 V | | 15 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

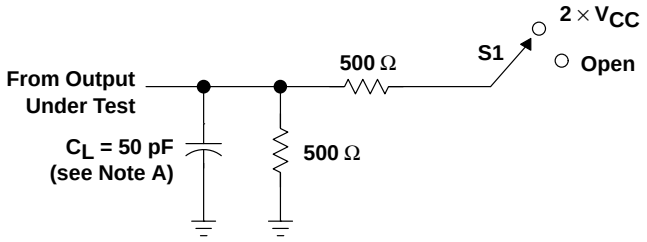
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | SN54ACT245 | | SN74ACT245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1 | 4 | 7.5 | 1 | 9 | 1.5 | 8 | ns |
| $t_{PHL}$ | | | 1 | 4 | 8 | 1 | 10 | 1 | 9 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1 | 5 | 10 | 1 | 12 | 1.5 | 11 | ns |
| $t_{PZL}$ | | | 1 | 5.5 | 10 | 1 | 13 | 1.5 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1 | 5.5 | 10 | 1 | 12 | 1 | 11 | ns |
| $t_{PLZ}$ | | | 1 | 5 | 10 | 1 | 12 | 1.5 | 11 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

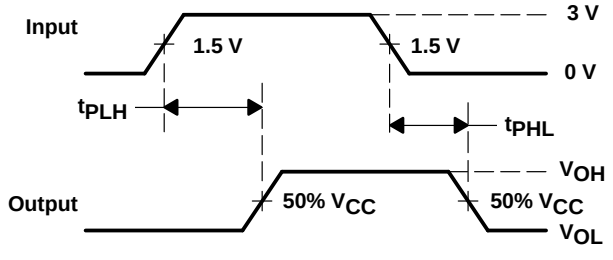
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ Power dissipation capacitance per transceiver | $C_L$ = 50 pF, f = 1 MHz | 45 | pF |

## PARAMETER MEASUREMENT INFORMATION

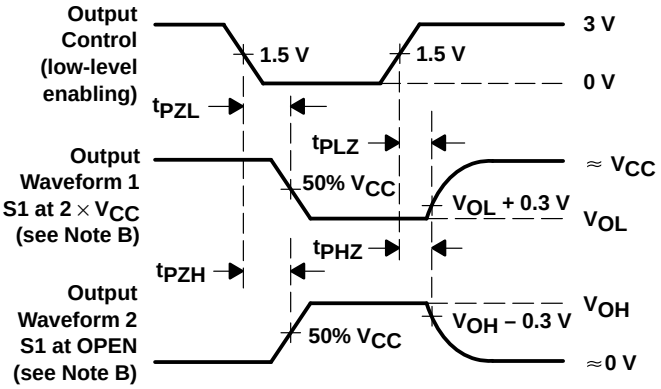



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open |

LOAD CIRCUIT




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.