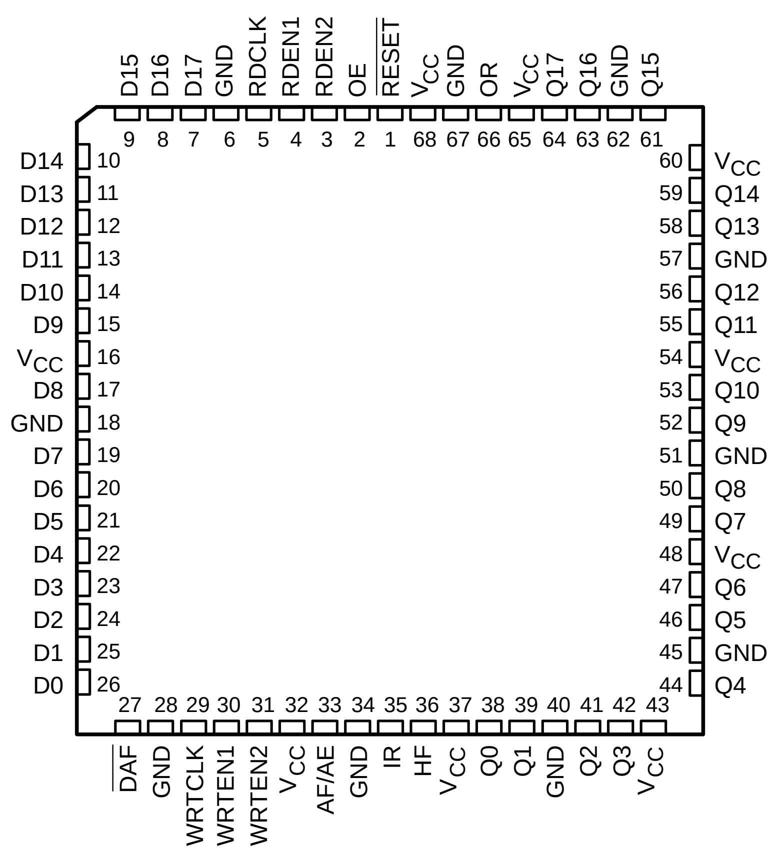
- **Members of the Texas Instruments Widebus™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **Read and Write Operations Can Be Synchronized to Independent System Clocks**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Pin-to-Pin Compatible With SN74ACT7881, SN74ACT7882, and SN74ACT7811**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 11 ns With a 50-pF Load**
- **High Output Drive for Direct Bus Interface**
- **Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat (PN) Packages**

FN PACKAGE
(TOP VIEW)

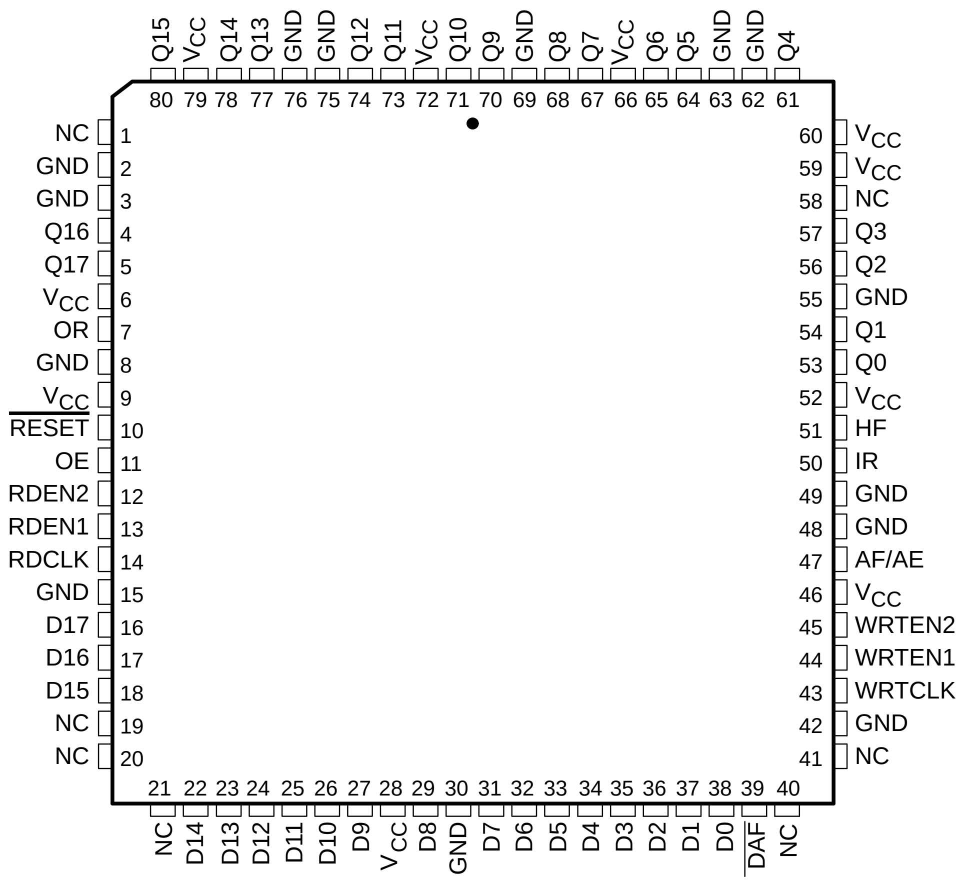


PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

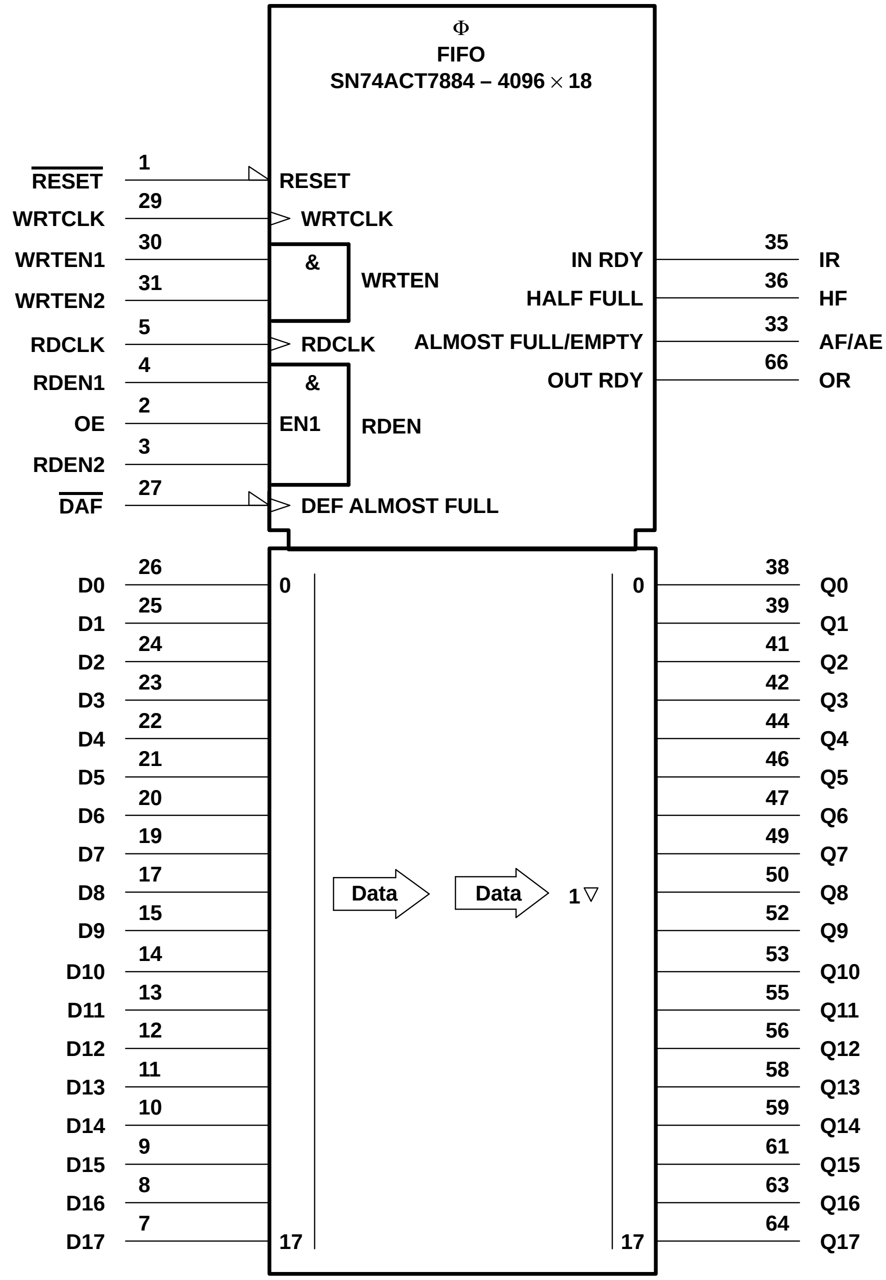
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7884 is organized as 4096 × 18 bits. The SN74ACT7884 processes data at rates up to 67 MHz and access times of 11 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7884 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent reads and writes to their respective system clocks.

The SN74ACT7884 is characterized for operation from 0°C to 70°C.

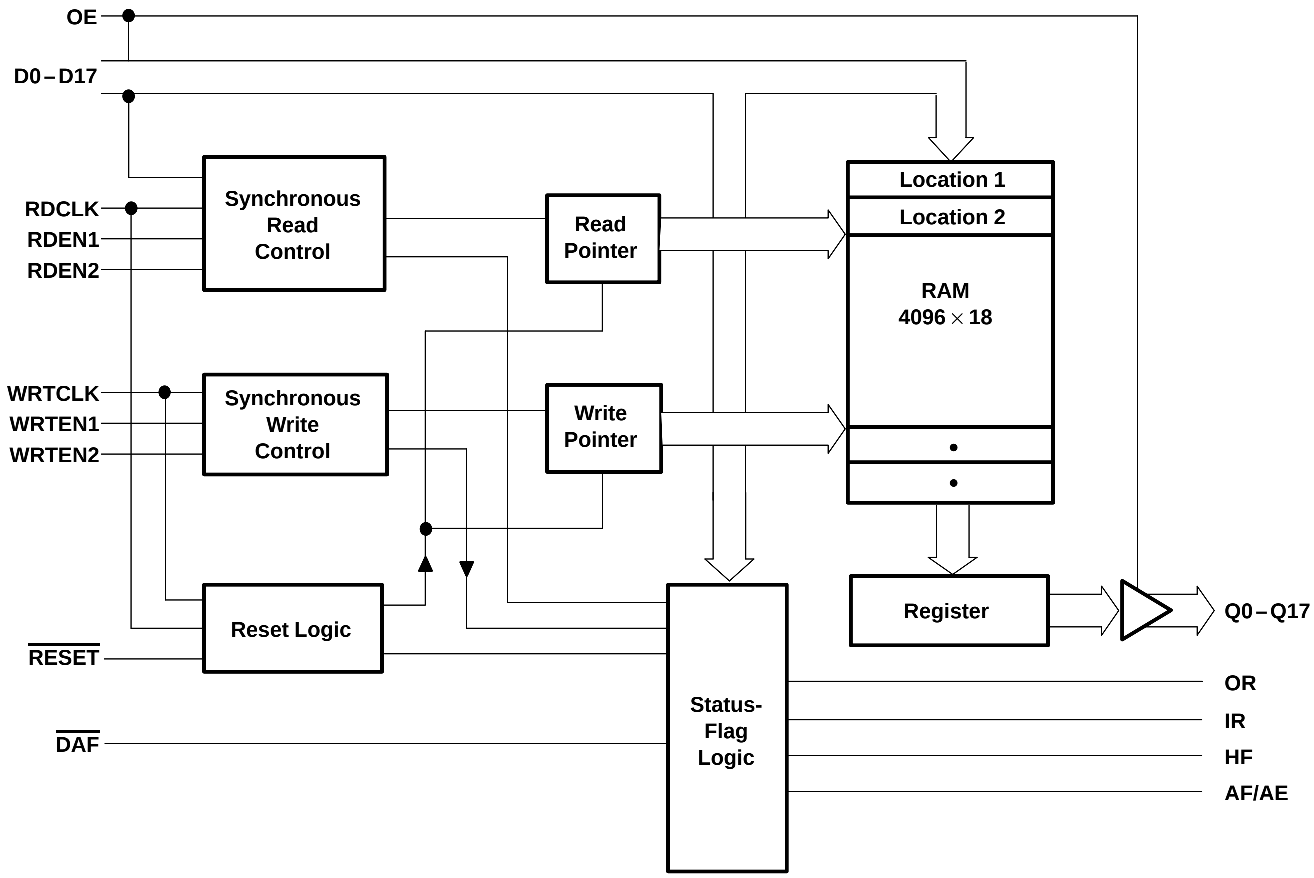
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

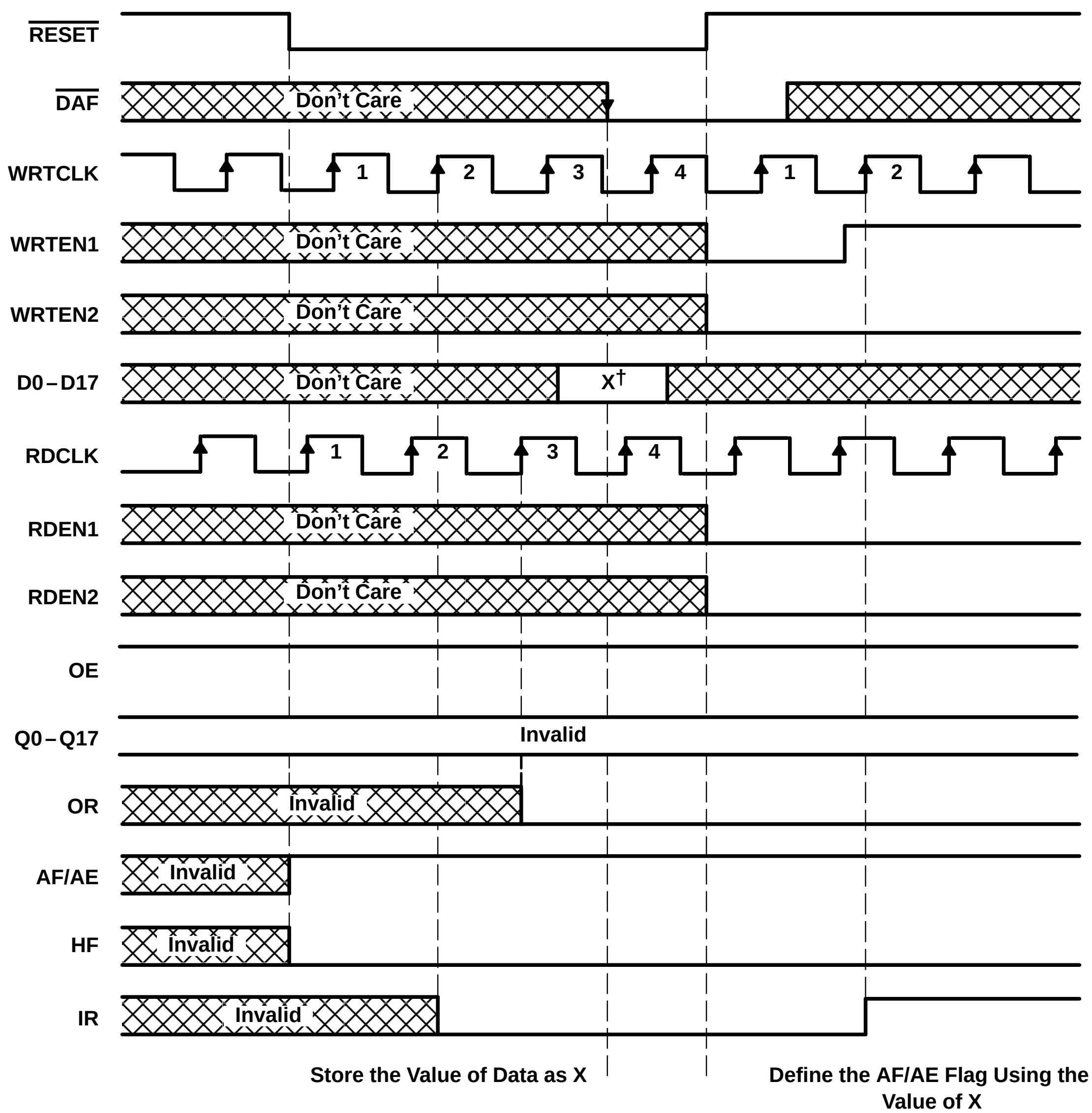
Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the number of words in memory is less than or equal to X. AF/AE is also high when the number of words in memory is greater than or equal to (4096 – X). Programming procedure for AF/AE is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: User-defined X Step 1: Take $\overline{\text{DAF}}$ from high to low. The low-to-high transition of $\overline{\text{DAF}}$ stores the binary value on the data inputs as X. The following bits are used, listed from most significant bit to least significant bit D10–D0. Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. Default X To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	27	I	Define-almost-full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the almost-full/almost-empty (AF/AE) flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. A high-to-low transition on $\overline{\text{DAF}}$ captures data for the almost-empty/almost-full offset (X) from D10–D0.
HF	36	O	Half-full flag. HF is high when the FIFO contains 2048 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The Q0–Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data out. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on the low-to-high transition at RDCLK if OR, OE, RDEN1, and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	1	I	Reset. A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, and IR are low, and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines AF/AE using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines AF/AE using the default value of X = 256.

PRODUCT PREVIEW

Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30, 31	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).



† X is the binary value on D10 – D0.

Figure 1. Reset Cycle: Define AF/AE Using a Programmed Value of X

PRODUCT PREVIEW

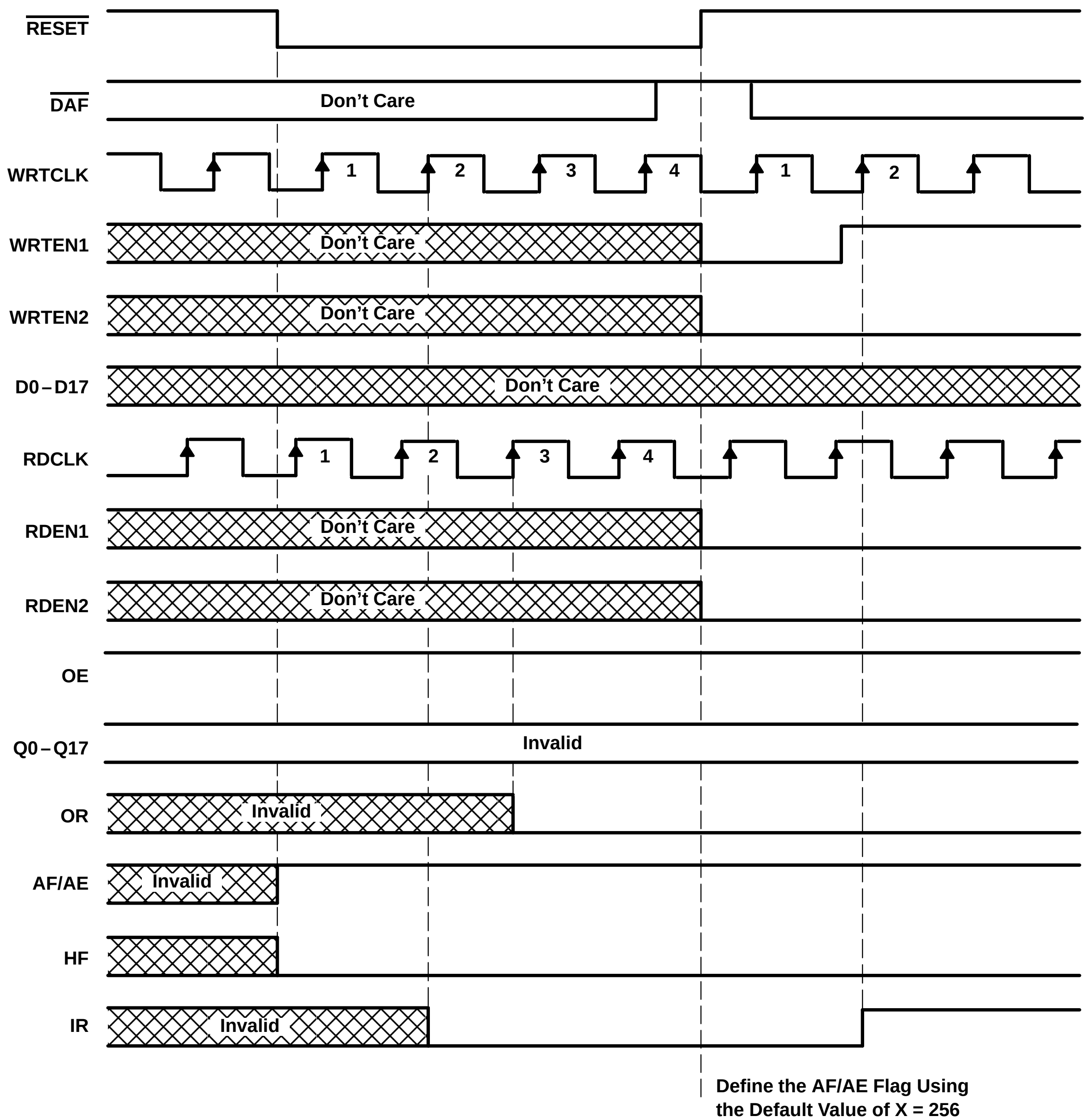
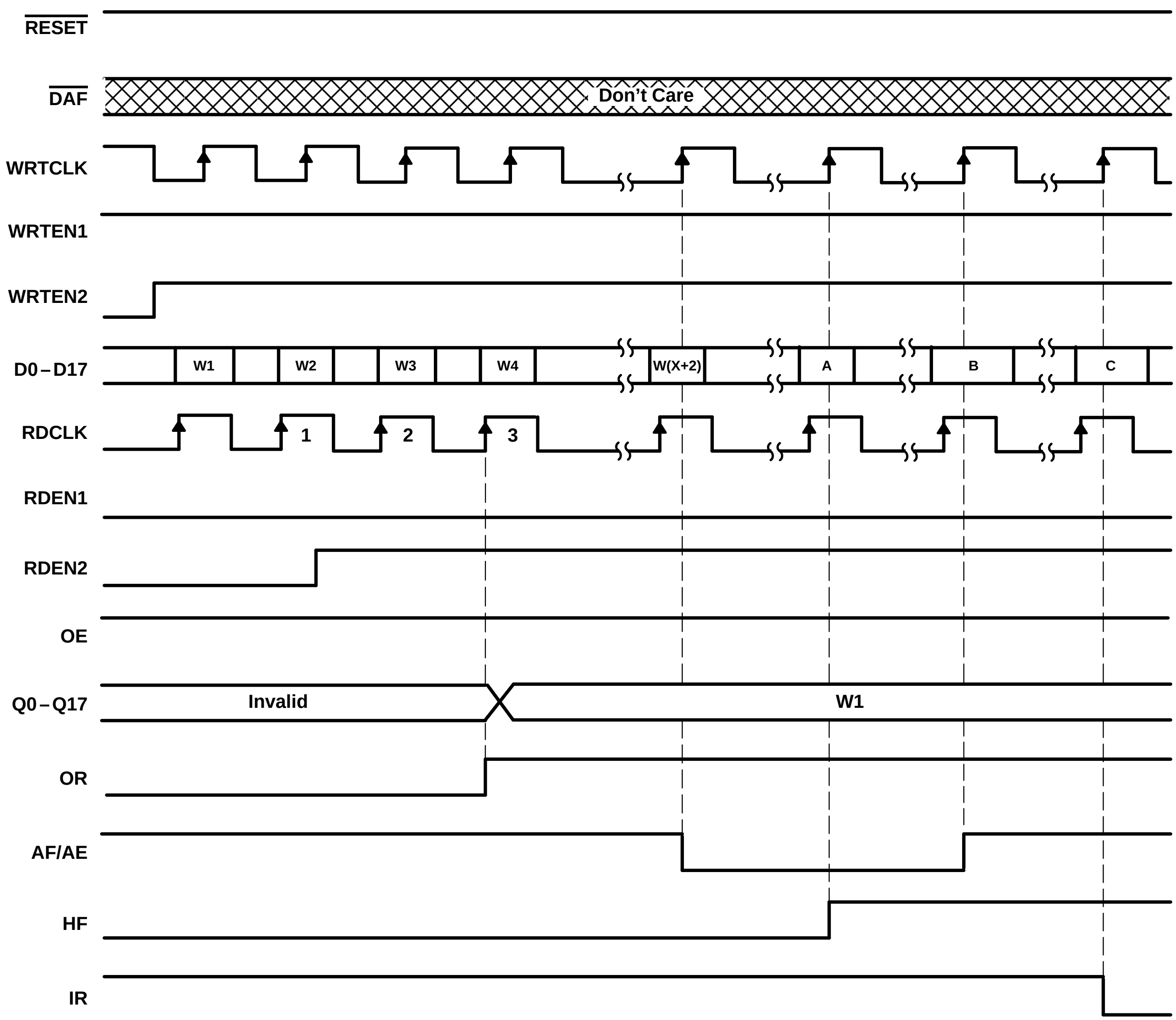


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

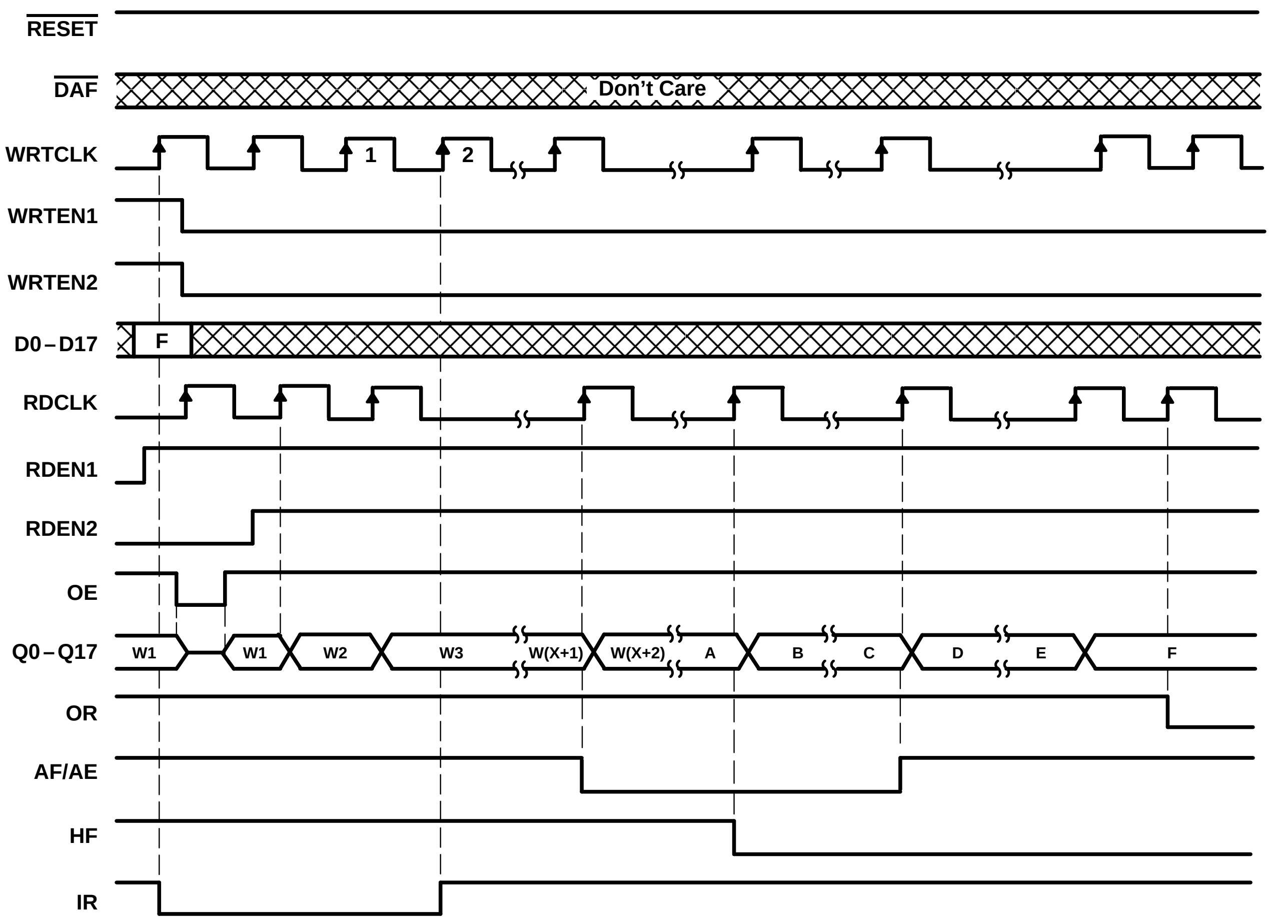
PRODUCT PREVIEW



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD		
A	**B**	**C**
W2049	W(4097 – X)	W4097

Figure 3. Write



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD					
A	**B**	**C**	**D**	**E**	**F**
W2049	W2050	W(4096 – X)	W(4097 – X)	W4096	W4097

Figure 4. Read

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage, V_I . . . . 7 V
Voltage applied to a disabled 3-state output . . . . 5.5 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	µA
I_{CC}§	V_I = V_{CC} – 0.2 V or 0				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz		4		pF
C_o	V_O = 0,	f = 1 MHz		8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} tested with outputs open.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 4)

			′ACT7884-15		′ACT7884-20		′ACT7884-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		33.4		MHz
t_w	Pulse duration	WRTCLK high	6		7		8.5		ns
		WRTCLK low	6		7		11		
		RDCLK high	6		7		8.5		
		RDCLK low	6		7		11		
		$\overline{DAF}$ high	6		7		10		
t_{su}	Setup time	Data in (D0–D17) before WRTCLK↑	4		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	4		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	4		5		5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	5		6		7		
		Define AF/AE: D0–D8 before $\overline{DAF}$↓	4		5		5		
		Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑	5		6		7		
		Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑	4		5		5		
t_h	Hold time	Data in (D0–D17) after WRTCLK↑	0		0		0		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	0		0		1		
		OE, RDEN1, RDEN2 high after RDCLK↑	0		0		1		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	0		0		0		
		Define AF/AE: D0–D8 after $\overline{DAF}$↓	0		0		1		
		Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑	0		0		0		
		Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑	0		0		1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 7 and 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	′ACT7884-15		′ACT7884-20		′ACT7884-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67		50		33.4		MHz
t_{pd}	RDCLK↑	Any Q	4	11	4	13	4	18	ns
t_{pd}‡									
t_{pd}	WRTCLK↑	IR	2	9	2	9.5	2	12	ns
t_{pd}	RDCLK↑	OR	2	9	2	9.5	2	12	
t_{pd}	WRTCLK↑	AF/AE	6	17	6	19	6	22	ns
	RDCLK↑		6	17	6	19	6	22	
t_{PLH}	WRTCLK↑	HF	6	15	6	17	6	21	ns
t_{PHL}	RDCLK↑		6	15	6	17	6	21	
t_{PLH}	$\overline{RESET}$↓	AF/AE	3	16	3	17	3	21	ns
t_{PHL}		HF	4	18	4	19	4	23	
t_{en}	OE	Any Q	2	11	2	11	2	11	ns
t_{dis}			2	14	2	14	2	14	

‡ This parameter is measured with C_L = 30 pF (see Figure 5).

PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

**PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE**

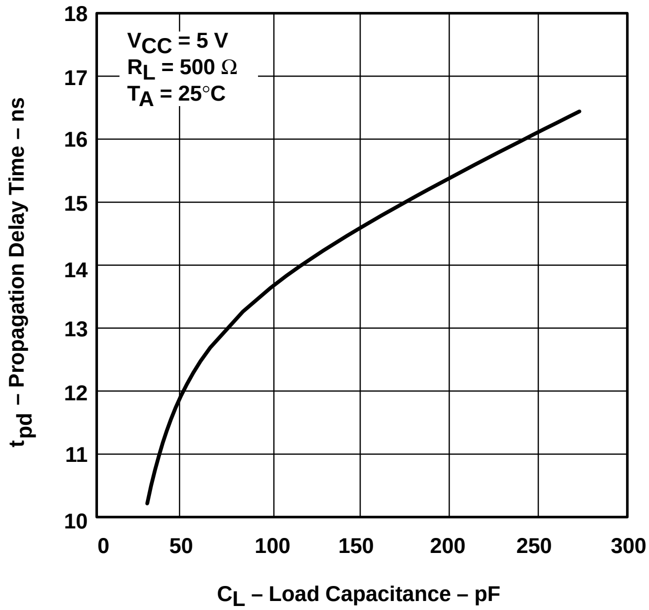


Figure 5

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

POWER DISSIPATION CAPACITANCE vs SUPPLY VOLTAGE

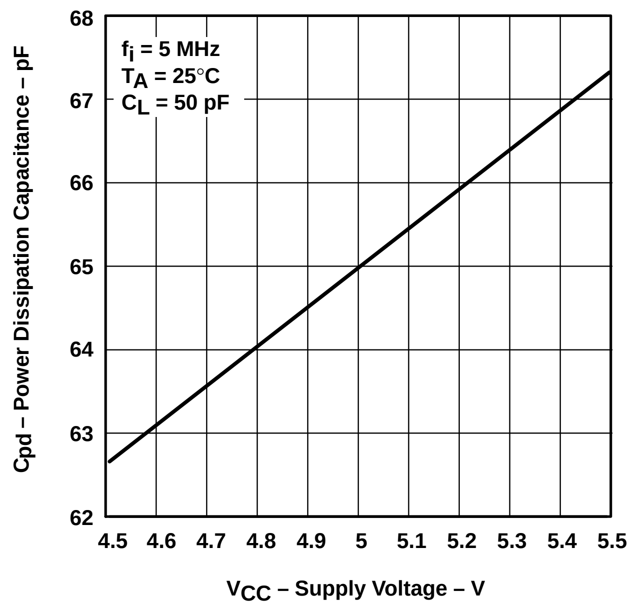


Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7884 can be calculated using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

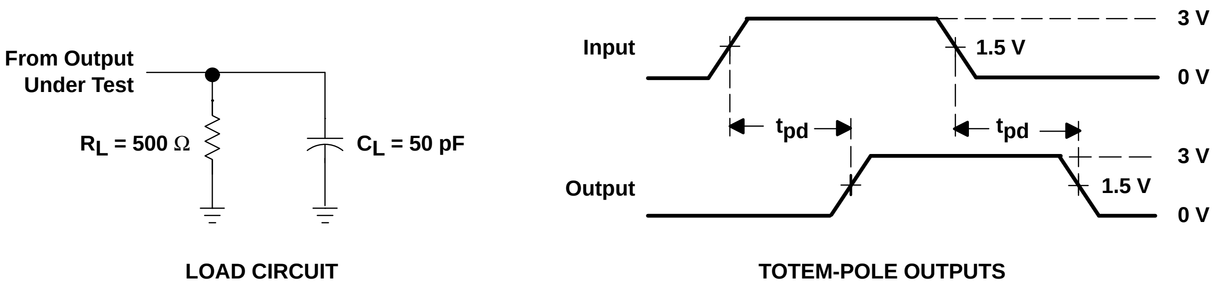
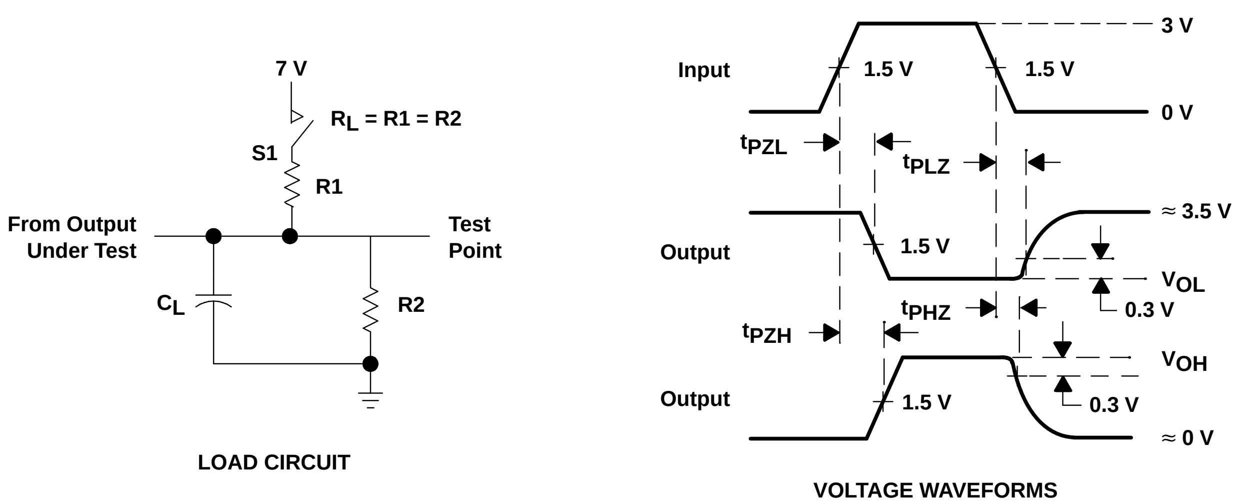


Figure 7. Standard CMOS Outputs



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 8. 3-State Outputs (Any Q)

APPLICATION INFORMATION

expanding the SN74ACT7884

The SN74ACT7884 is expandable in both word width and word depth. Word-depth expansion is accomplished by connecting the devices in series such that data flows through each device in the chain. Figure 9 shows two SN74ACT7884 devices configured for depth expansion. The common clock between the devices can be tied to either the write clock (WRTCLK) of the first device or the read clock (RDCLK) of the last device. The output-ready flag (OR) of the previous device and the input-ready flag (IR) of the next device maintain data flow to the last device in the chain whenever space is available.

Figure 10 is an example of two SN74ACT7884 devices in word-width expansion. Width expansion is accomplished by simply connecting all common control signals between the devices and creating composite input-ready (IR) and output-ready (OR) signals. The almost-full/almost-empty flag (AF/AE) and half-full flag (HF) can be sampled from any one device. Depth expansion and width expansion can be used together.

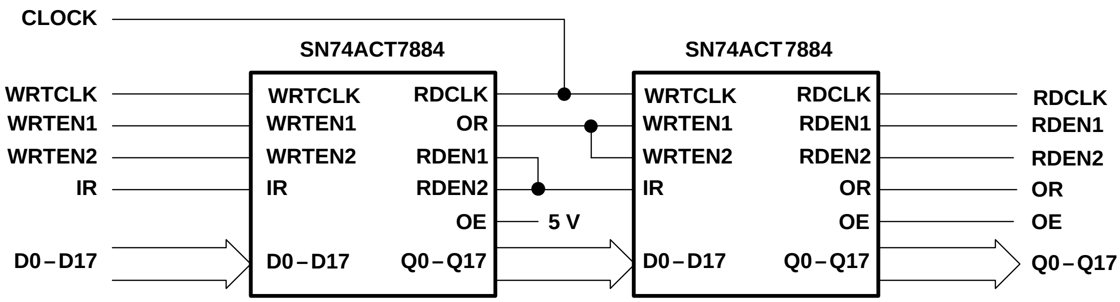


Figure 9. Word-Depth Expansion: 2048/4096/8192 Words × 18 Bits, N = 2

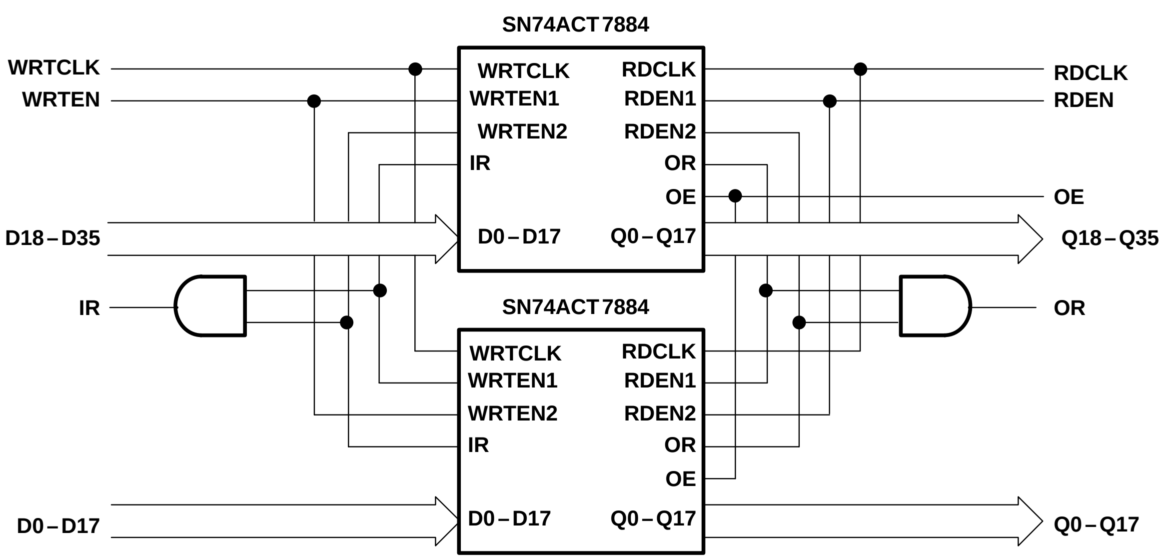


Figure 10. Word-Depth Expansion: 4096 Words × 36 Bits

PRODUCT PREVIEW

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