4096 × 18 CLOCKED MULTIPLE-QUEUE (MULTI-Q™) FIRST-IN, FIRST-OUT MEMORY WITH THREE PROGRAMMABLE-DEPTH BUFFERS AND CELL-BASED FLAGS

SCAS443A – JUNE 1994 – REVISED JULY 1995

- **4096 × 18 Total Memory Size**
- **Three Programmable-Depth FIFOs on One Device**
- **Memory Allocation of 256 × 18 Blocks**
- **Two Separate Read and Write Clocks That Can Operate Synchronously or Asynchronously**
- **Clocked Interface; Read and Write Enables Synchronize Data Transfers to Continuous Clocks**
- **Programmable Cell Size From 10 to 32 18-Bit Words**
- **Cell-Abort Feature to Discard a Previous Cell Write**
- **Cell-Ready Flag for Each Queue Synchronized to Read Clock**
- **Programmable Flag With Hysteresis for Each Queue Synchronized to Write Clock**
- **Last Word of Cell Flag Synchronized to Read Clock**
- **Input or Output Bus Size of 9 Bits or 18 Bits, Byte Stuff/Destuff Capability**
- **Data Access Times of 11 ns**
- **Synchronous Multiplexer for Queue Output Selection**
- **8-bit Bidirectional Programming Port**
- **Clock Frequencies up to 50 MHz**
- **Produced in 0.8-μm Advanced CMOS Technology**
- **Available in 100-Pin Thin Quad Flat (PZ) Package**

description

The Multi-Q FIFO is a first-in, first-out (FIFO) memory with three programmable-length queues and a total memory size of 4096 words of 18 bits each to provide two or three quality of service (QOS) bins for ATM traffic in a single device. The core memory is divided into sixteen 256 x 18 blocks that can be allocated to each queue according to the user's need.

Flags for the queues are designed to indicate the presence or absence of entire cells rather than individual words. The number of 18-bit words that constitutes one cell is programmable by the user and has a default value of 27. A cell-ready (CR) flag for a queue is high when at least one complete cell is present in the queue. Each CR flag is synchronized to the read clock (RDCLK). The full flag ($\overline{FF}$) for each queue is synchronized to the write clock (WRTCLK) and indicates when no more cells can be written to the queue. A programmable flag (PF) is provided for each queue, which is synchronized to the WRTCLK. Each PF has two programmable values. PF is low when the number of cells in the queue are greater than or equal to the first limit, and it is set high when the number of cells in the queue are reduced to the second limit. This allows the user to define a hysteresis threshold for the flag if it is needed.

WRTCLK and RDCLK are designed to be free-running clock inputs to maintain the proper synchronization of the flags. The clocks are synchronized or asynchronous in phase, frequency, or both. Writes to one of the three queues is done by a rising edge of WRTCLK when the queue's write enable (WRTEN) is high. Any write can be done to two or three of the queues simply by asserting two or three of the WRTEN inputs for a WRTCLK rising edge. Data is read from a queue by the rising edge of RDCLK when the queue is selected by the multiplexer (MUX0, MUX1) inputs and the read enable (RDEN) is high. Configuration registers can be programmed to set the input or output port sizes to 9 bits or 18 bits. Big- or little-endian data format can be selected for the buses. When matching 9-bit buses to 18-bit or 36-bit buses with the Multi-Q, byte stuffing can be selected for the data input and byte destuffing can be done on the data output.

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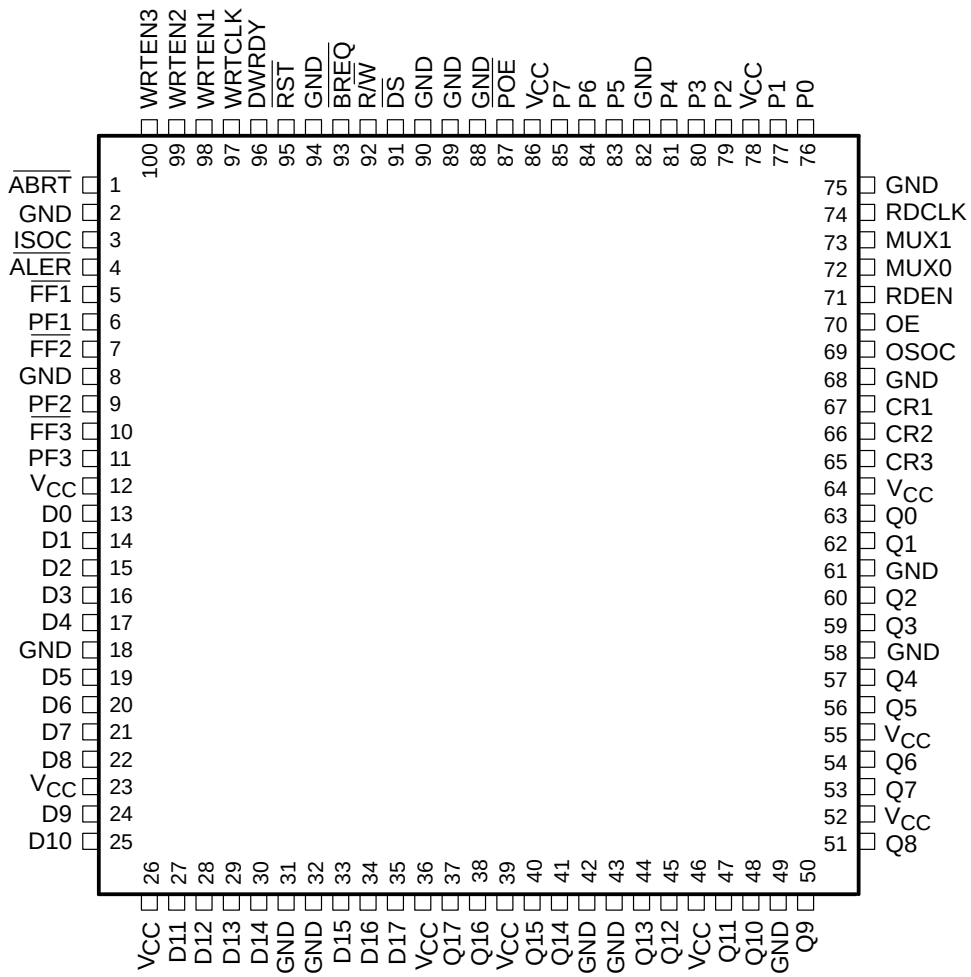
PZ PACKAGE
(TOP VIEW)



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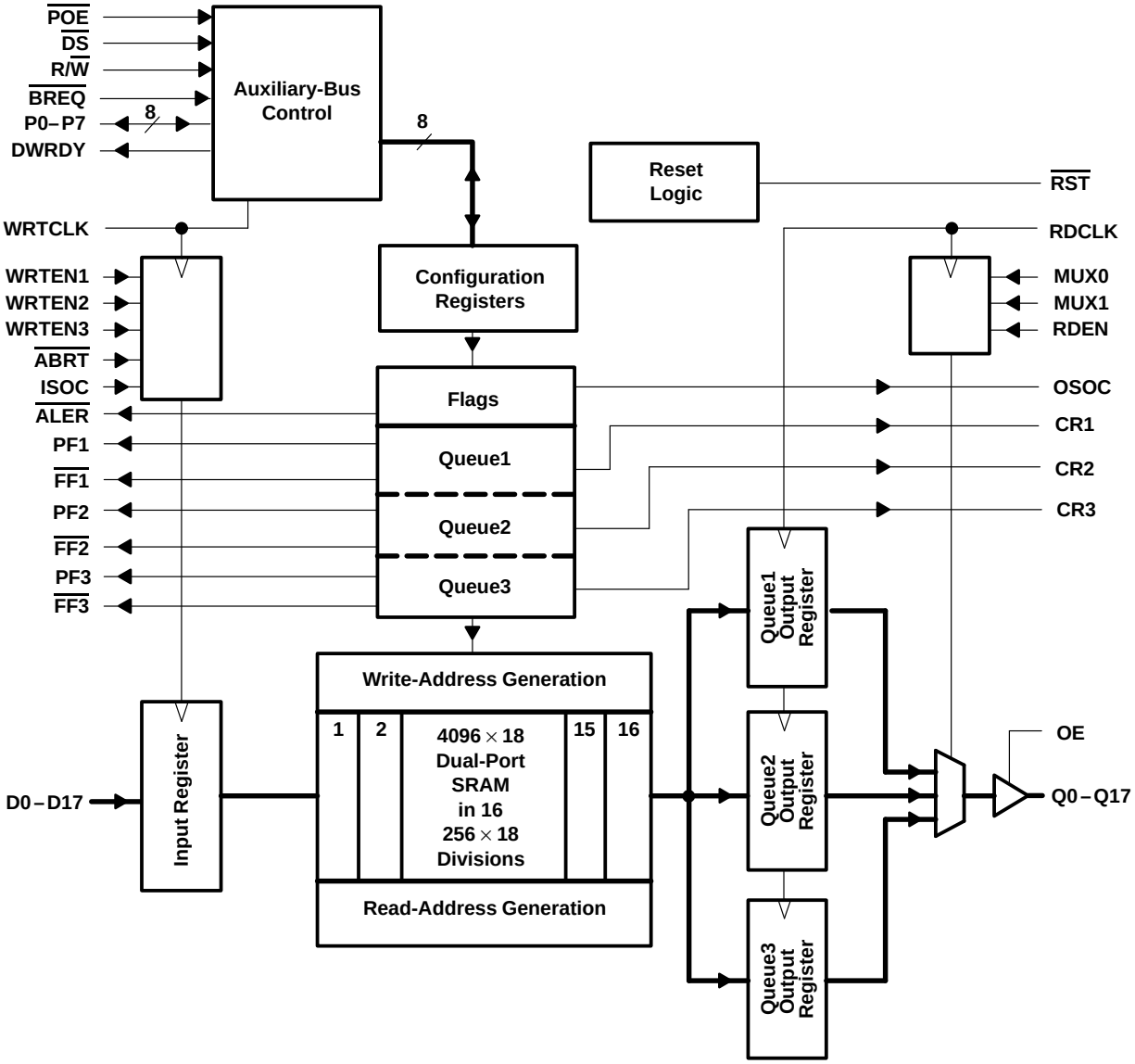
functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
$\overline{\text{ABRT}}$	I	Abort. When $\overline{\text{ABRT}}$ is held low, all data stored since the queue's last cell-abort marker are discarded.
$\overline{\text{ALER}}$	O	Align error. $\overline{\text{ALER}}$ maintains cell synchronization at the input. If ISOC and internal start-of-cell status disagree, $\overline{\text{ALER}}$ is low and writes are disabled.
$\overline{\text{BREQ}}$	I	Bus request. When $\overline{\text{BREQ}}$ is low, DWRDY is set low and writes are performed to the configuration registers. When $\overline{\text{BREQ}}$ is high, DWRDY is set high and writes are performed to the 18-bit input port.
$\overline{\text{CR}}$	O	Cell-ready flag. $\overline{\text{CR}}$ for each queue is high when at least one complete cell is present in the queue. $\overline{\text{CR}}$ is set low upon the read of the last word or byte in a cell, if no other complete cells are stored in the FIFO.
D0–D17	I	18-bit data input port
$\overline{\text{DS}}$	I	Data strobe. A high-to-low transition of $\overline{\text{DS}}$ latches the data on the 8-bit programming bus to the configuration registers. A low-to-high transition of $\overline{\text{DS}}$ sends the data from configuration registers to the programming bus.
DWRDY	O	Data-write ready. DWRDY gives control of data writing to the input bus or the 8-bit programming bus. Data writes to the programming bus are allowed when DWRDY is low and data writes to the synchronous bus are allowed when DWRDY is high.
$\overline{\text{FF}}$	O	Full flag. Full flag for each queue is synchronized to the WRTCLK. When $\overline{\text{FF}}$ is low, no more cells can be written to the FIFO. $\overline{\text{FF}}$ is set high by the second low-to-high transition of WRTCLK after the last byte or word read of a cell in the queue.
ISOC	I	Input start of cell. ISOC must be high for the first word or byte write of a cell and low for all other word or byte writes.
MUX1, MUX0	I	Multiplexer inputs. MUX1 and MUX0 select one of the three queues output registers.
OE	I	Output enable. Q0–Q17 are in the high-impedance state when OE is low.
OSOC	O	Output start of cell. OSOC is high when the first word or byte of cell is present in the output register of the queue. When any other word or byte of a cell or invalid data is present in the output register of the queue, OSOC is low.
P0–P7	I/O	8-bit bidirectional programming bus
PF	O	Programmable flag. PF is low when the number of cells in the queue are greater than or equal to write threshold stored in the queue's PFX_W register. PF is set high when the number of cells in the queue are reduced to the read threshold stored in the queue's PFX_R register.
$\overline{\text{POE}}$	I	Program output enable. The programming bus (P0–P7) outputs are active when $\overline{\text{POE}}$ is low and R/$\overline{\text{W}}$ is high.
Q0–Q17	O	18-bit data output port
$\overline{\text{RST}}$	I	FIFO reset. To reset FIFO, four low-to-high transitions of WRTCLK and four low-to-high transition of RDCLK must occur while $\overline{\text{RST}}$ is low.
RDCLK	I	Read clock. RDCLK is a continuous clock and is asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from a queue when the queue is selected by MUX0, MUX1 and RDEN is high.
R/$\overline{\text{W}}$	I	Read/write select. R/$\overline{\text{W}}$ high selects a read operation and low selects a write operation on the 8-bit programming bus.
RDEN	I	Read enable. RDEN high enables a low-to-high transition of the read clock to read data from the queue selected by MUX1 and MUX0.
WRTCLK	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to one of the 3 queues when WRTEN and $\overline{\text{FF}}$ are high.
WRTEN	I	Write enable. A queue's WRTEN must be high to enable a low-to-high transition of WRTCLK to write data to the queue.

detailed description

reset

The Multi-Q FIFO is reset by setting the reset ($\overline{RST}$) input low for four WRTCLK and four RDCLK low-to-high transitions. When the device is reset, the cell ready (CR1, CR2, and $\overline{CR3}$) flags for each queue are set low, the programmable flags (PF1, PF2, and PF3) are set high, the full flags ($\overline{FF1}$, $\overline{FF2}$, and $\overline{FF3}$) are set high, the align error ($\overline{ALER}$) is set high, and the output start of cell (OSOC) is set low. During a device reset, the default values shown in Table 1 are loaded into the configuration registers.

Table 1. Configuration Registers

REGISTER SYMBOL	REGISTER NAME	NO. OF BITS	DEFAULT VALUE	PROGRAMMABLE RANGE	FUNCTION
PORT	Port Control	5	0	Bit-slice control	Chooses the data input and output bus size and format. Controls output byte destuffing.
QL1	Queue1 Length	5	8	0–16	Defines number of 256 × 18 memory blocks allocated to Queue1
QL2	Queue2 Length	4	6	0–15	Defines number of 256 × 18 memory blocks allocated to Queue2
QL3	Queue3 Length	4	2	0–15	Defines number of 256 × 18 memory blocks allocated to Queue3
CLSZ	Cell Size	6	27	10–32	Defines the number of 18-bit words in one cell
PF1_W	Programmable Flag 1, Write Threshold	9	71	1–409	Defines the number of cells stored in Queue1 to set PF1 low
PF1_R	Programmable Flag 1, Read Threshold	9	70	0–408	Defines the number of cells stored in Queue1 to reset PF1 high
PF2_W	Programmable Flag 2, Write Threshold	9	51	1–383	Defines the number of cells stored in Queue2 to set PF2 low
PF2_R	Programmable Flag 2, Read Threshold	9	50	0–382	Defines the number of cells stored in Queue2 to reset PF2 high
PF3_W	Programmable Flag 3, Write Threshold	8	13	1–383	Defines the number of cells stored in Queue3 to set PF3 low
PF3_R	Programmable Flag 3, Read Threshold	8	12	0–382	Defines the number of cells stored in Queue3 to reset PF3 high

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default values for the configuration registers

Port Control:

A 4-bit register that controls the sizing and word-align functions of the input and output data ports. Figure 1 shows the bit configuration of the port-control register. Table 2 lists the register bits, names, and functions.

4	3	2	1	0
OUTSTF	OUTSIZ	INSTF	INBE	INSIZ

Figure 1. Port-Control Register

default values for the configuration registers (continued)

Table 2. Port-Control Register Bits

BIT	NAME	VALUE	FUNCTION
0	INSIZ	0 (default value)	Enables an 18-bit input data bus
		1	Enables a 9-bit input data bus
1	INBE	0 (default value)	Enables the placement of D0–D8 data in memory with a little-endian format if INSIZ bit is a 1
		1	Enables the placement of D0–D8 data in memory with a big-endian format (INSIZ bit is a 1)
2	INSTF	0 (default)	Sets the end of a cell write to be the last byte write of the last word as defined by the cell size (CLSZ) register if INSIZ bit is a 1
		1	Sets the end of a cell write to be the first byte write of the last word and the byte write is copied to both bytes of the word (INSIZ bit is a 1)
3	OUTSTF	0 (default)	Enables 18-bit data output
		1	Enables 9-bit data output
4	OUTSTF	0 (default)	Allows byte reads to precede normally on all words of a cell (OUTSIZ bit is a 1)
		1	After the first byte of the last word of a cell is read, the last byte of the last word of that cell is ignored and the first byte of the first word of the subsequent cell is read (OUTSIZ bit is a 1).

Queue Length:

The three queue-length registers (QL1, QL2, and QL3) have default values of 8, 6, and 2, respectively. This defines the 18-bit wide Queue1 memory depth as 2048 (8 x 256); Queue2 memory depth as 1536 (6 x 256); and Queue3 memory depth as 512 (2 x 256). The QL1 register has five bits and can be programmed to utilize the entire memory of the device for Queue1.

Cell Size:

The cell-size register (CLSZ) has a default value of 27. This defines 27 18-bit words as one cell for the cell-ready flags and programmable flags.

Programmable-Flag Write Threshold:

The default values for the PF1_W, PF2_W, and PF3_W registers are chosen to set the respective programmable flags low when the number of 27-word cells stored in its queue is five cells from filling its buffer.

Programmable-Flag Read Threshold:

The default values for the PF1_R, PF2_R, and PF3_R registers are chosen to reset the respective programmable flags high when the number of 27-word cells stored in its queue is reduced by (PF1_W)–1, (PF2_W)–1, (PF3_W)–1.

data writes

Data writes are synchronized to the write clock (WRTCLK) and can occur asynchronous to the read clock (RDCLK) while any of the three queues are being read. The data-write-ready (DWRDY) output must be high to allow a data write from the data inputs (D0–D17) into one or more of the queue memories. When DWRDY is high, the low-to-high transition of WRTCLK stores data (D0–D17) in Queue1 when the WRTEN1 input is high and the $\overline{FF1}$ output is high, Queue2 when the WRTEN2 input is high and the $\overline{FF2}$ output is high, and Queue3 when the WRTEN3 input is high and the $\overline{FF3}$ output is high. Data can be stored in two or three queues simultaneously by asserting two or three WRTEN signals.

The input start-of-cell (ISOC) input and the align-error ($\overline{ALER}$) output are used to maintain cell synchronization at the input of the device. The ISOC should be high for the first word or byte write of a cell and should be low for all other word or byte writes of the cell. The SN74ACT53861 maintains its own start-of-cell status and compares this to the ISOC on each word or byte write. If a word or byte write is attempted when the ISOC and the internal start-of-cell status disagree, the write is prevented and $\overline{ALER}$ is set low.

data writes (continued)

When all words of a cell are successfully written to one of the queues, the queue flags are updated. In addition to updating the queue flags, a completed cell write moves the cell-abort marker to the next memory write location in the queue. After a reset, the cell-abort marker for each queue is positioned at the first memory write location.

If a 9-bit data input is selected by the port-control register, data is input to the FIFO through bits D0–D8. If the INBE bit of the PORT register is set to 1, data is stacked into memory big-endian style with the first byte write of a word stored in the D9–D17 byte and the second byte write of a word stored in the D0–D8 byte. If INBE is set to 0, little-endian stacking is enabled with the first byte write of a word stored in the D0–D8 byte and the second byte write of a word stored in the D9–D17 byte.

All data writes since a queue's last cell-abort marker are discarded when the abort ($\overline{\text{ABRT}}$) input is held low and the queue's write enable (WRTEN1, WRTEN2, or WRTEN3) is held high for a low-to-high transition of WRTCLK. The internal write pointer for the queue memory is set to the cell-abort marker for the queue, discarding all data written since the last cell completion. No data write is performed during the abort cycle.

data reads

Data reads are synchronized to the read clock (RDCLK) and can occur asynchronous to the write clock (WRTCLK) while any of the three queues are being written. A data read is done on a queue by the low-to-high transition of RDCLK when the queue is selected by the multiplexer (MUX0, MUX1) inputs (see Table 3), the read enable (RDEN) input is high, and the cell-ready-flag (CR1, CR2, or CR3) output for the queue is high.

Table 3. Output-Queue Selection by Multiplexer Inputs

MUX1	MUX0	QUEUE OUTPUT
0	0	Queue1
0	1	Queue1
1	0	Queue2
1	1	Queue3

The status of the OUTSIZ bit in the PORT register determines if the output data bus size is 18-bit word or 9-bit byte. If OUTSIZ is 0, each read outputs a new queue word on Q0–Q17. If OUTSIZ is 1, the first read outputs a new queue word on Q0–Q17 and the next read swaps the byte order of Q0–Q8 and Q9–Q17. This pattern is repeated for each subsequent word read.

If the OUTSTF bit in the PORT register is a 1 and the OUTSIZ bit is a 1, the first byte read of the last word of a cell completes the cell read and the next byte read outputs a new word on the data bus, discarding the last byte of each cell. No change in data output flow occurs if OUTSTF is a 0.

The cell-ready flag and programmable flag for each queue are updated upon the read of the last word of a cell. The number of words in a cell is defined by the contents of the cell-size (CLSZ) configuration register. When the output-data-bus size is byte and the OUTSTF bit is a 0, the last byte read of the last word of a cell updates the flags. If OUTSTF bit is a 1, the first byte read of the last word of a cell updates the flags.

The output-start-of-cell (OSOC) output is high when the first word or byte of a cell is present in the output register of the queue selected by the MUX1 and MUX0 inputs. When any other word or byte of a cell is present in the output register of the queue selected by the MUX1 and MUX0 outputs or if the contents of the selected register is invalid, the OSOC is low. OSOC is synchronous to the low-to-high transition of RDCLK.

Switching queues for data output is done synchronous to the low-to-high transition of RDCLK. If RDEN and the cell-ready flag are high at the time the queue output switch occurs, a read is done on the new queue. If RDEN is low at the time the queue output switch occurs, the previously read data value held in the new queue's output register is output on Q0–Q17. Queue switching should only be performed on cell boundaries.

data reads (continued)

OE controls the state of the data outputs (Q0−Q17). When OE is high, Q0−Q17 are active. When OE is low, Q0−Q17 are in the high-impedance state.

cell-ready flags

Each queue has a cell-ready flag (CR1, CR2, or CR3) that is high when at least one complete cell is stored in the queue. The cell-ready flags are synchronized to the low-to-high transition of the RDCLK. After reset, the cell-ready flags are set low. The low-to-high transition of a queue's cell-ready flag is initiated when a cell write to an empty queue is complete. The queue's cell-ready flag is set high by the second RDCLK rising edge after this event. The cell-ready flag is set low upon the read of the last word or byte in a cell if no other complete cells are loaded in the queue. Reads from a queue are inhibited while its cell-ready flag is low.

full flags

Each queue has a full flag ($\overline{FF1}$, $\overline{FF2}$, or $\overline{FF3}$) that is set high when at least one complete cell space is available in the queue. Upon programming the queue length and the cell size, the SN74ACT53861 calculates the maximum number of complete cells which can be written to a queue. When the number of cells stored in a queue is equal to this maximum value, the queue's full flag is set low. full flags are synchronous to the low-to-high transition of the WRTCLK. When a queue's full flag is low, the full flag is set high by the second WRTCLK low-to-high transition after the last byte or word read of a cell in the queue.

programmable flags

Each queue has one programmable flag (PF1, PF2, or PF3) that is synchronized to the low-to-high transition of the WRTCLK. Two registers per queue define the boundaries of the programmable flags; the write threshold register (PF1_W, PF2_W, or PF3_W) and the read threshold register (PF1_R, PF2_R, or PF3_R). When the word write that stores the number of complete cells equals the queue's PFx_W register, its programmable flag is set low. The low-to-high transition of the programmable flag is initiated by the read of the last word or byte in a cell. This reduces the number of stored cells equal to the queue's PFx_R value. The programmable flag is set high by the second WRTCLK low-to-high transition after this event.

programming the configuration registers

The configuration registers for the Multi-Q FIFO can be programmed after a device reset and before data is written to one of the queues. The programming port (P0−P7) is used to sequentially write or read the configuration registers.

In order to write to the configuration registers, control of the bus must first be acquired by asserting the bus-request ($\overline{BREQ}$) input low, which in turn sets the data write ready (DWRDY) output low after two rising edges of WRTCLK. DWRDY gives data-writing control to the synchronous input bus (WRTCLK, WRTEN1–3, D0−D17) or the 8-bit programming bus. Data writes to the programming bus are allowed when DWRDY is low and data writes to the synchronous input bus are allowed when DWRDY is high. Data on P0−P7 is written to the configuration registers on the high-to-low transition of data strobe ($\overline{DS}$) when DWRDY is low and the read/write (R/$\overline{W}$) input is low. The configuration registers are written in the sequence shown in Table 4. Ten writes are needed to program the configuration registers. After all ten registers are programmed, further data-write attempts to the configuration registers are ignored until the device is reset again. When programming is complete, $\overline{BREQ}$ is set high to set DWRDY high and returns input control to the 18-bit synchronous input port. A list of rules for configuration register programming follows.

Rules for queue length (QL1, QL2, QL3) register values:

Zero is the minimum value.

Sixteen is the maximum value for QL1. Fifteen is the maximum value for QL2 and QL3.

Only QL1 and QL2 can be programmed by the user. QL3 is calculated by the device to use the remaining memory (if any exists).

programming the configuration registers (continued)

Rules for cell-size (CS) register values:

Ten is the minimum value.

Thirty-two is the maximum value.

Rules for programmable-flag write-threshold (PF1_W, PF2_W, and PF2_W) register values:

One is the minimum value.

Value must not exceed number of complete cells that can be stored in the buffer defined by its queue length register and the cell-size register.

The PF1_W, PF2_W, and PF3_W registers are nine bits each. The most significant eight bits are programmable by the user and the least significant bit is always a 1; therefore, PFx_W values are odd.

Rules for programmable-flag read-threshold (PF1_R, PF2_R, and PF3_R) register values:

Zero is the minimum value.

Value must be less than the corresponding programmable-flag write-threshold register value.

The PF1_R, PF2_R, and PF3_R registers are nine bits each. The most significant eight bits are programmable by the user and the least significant bit is always 0; therefore, all PFx_R values are even.

Table 4. Accessing Configuration Registers From the Programming Bus for Data Writes

WRITE ORDER	REGISTER	PROGRAMMING BUS PORTS	
		MSB	LSB
1	PORT	P4	P0
2	QL1	P4	P0
3	QL2	P3	P0
4	CLSZ	P5	P0
5	PF1_W	P7	P0
6	PF1_R	P7	P0
7	PF2_W	P7	P0
8	PF2_R	P7	P0
9	PF3_W	P7	P0
10	PF3_R	P7	P0

The programming bus (P0–P7) is a bidirectional port whose outputs are active when the program-output-enable ($\overline{POE}$) input is low and the read/write (R/$\overline{W}$) input is high. When the P0–P7 outputs are active, data from the configuration registers are output. The next configuration register in sequence shown in Table 5 is sent to the programming-bus outputs on a low-to-high transition of $\overline{DS}$ when R/$\overline{W}$ is high. After all ten registers have been read in sequence, a subsequent programming-bus read accesses the PORT register again. Unused bit values for a register appear as logical 0 on the programming bus.

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programming the configuration registers (continued)

Table 5. Accessing Configuration Registers From the Programming Bus for Data Reads

WRITE ORDER	REGISTER	PROGRAMMING BUS PORTS	
		MSB	LSB
1	PORT	P3	P0
2	QL1	P4	P0
3	QL2	P3	P0
4	CLSZ	P5	P0
5	PF1_W	P7	P0
6	PF1_R	P7	P0
7	PF2_W	P7	P0
8	PF2_R	P7	P0
9	PF3_W	P7	P0
10	PF3_R	P7	P0

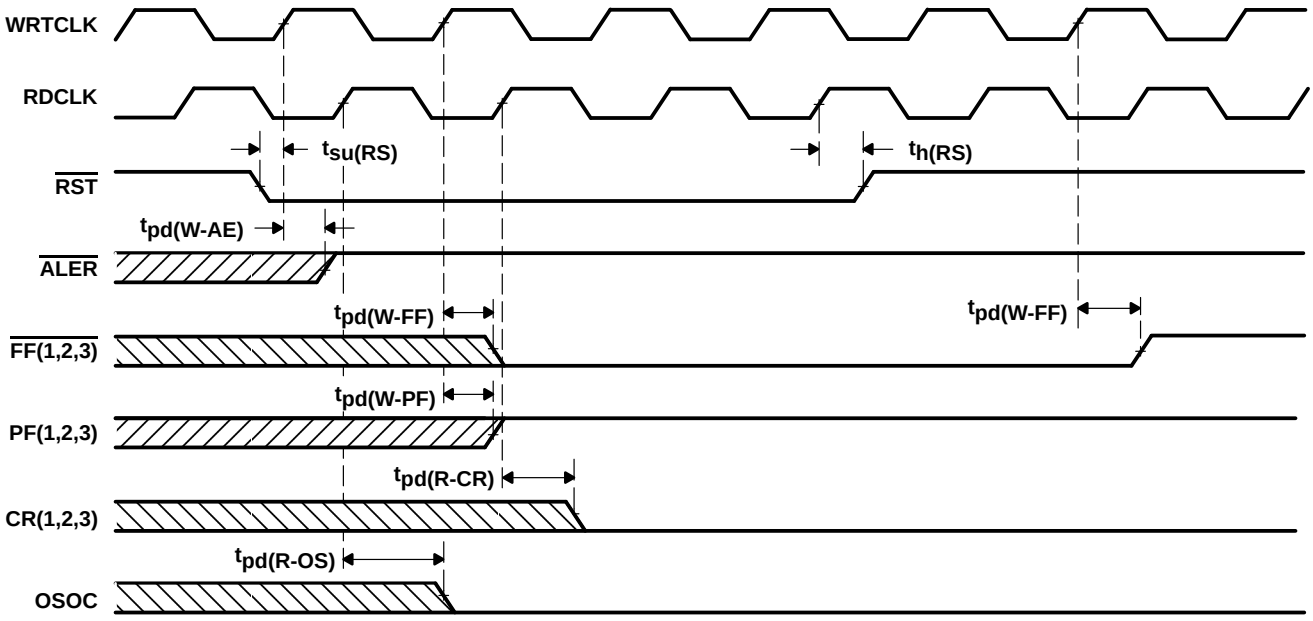

Figure 2. Device Reset

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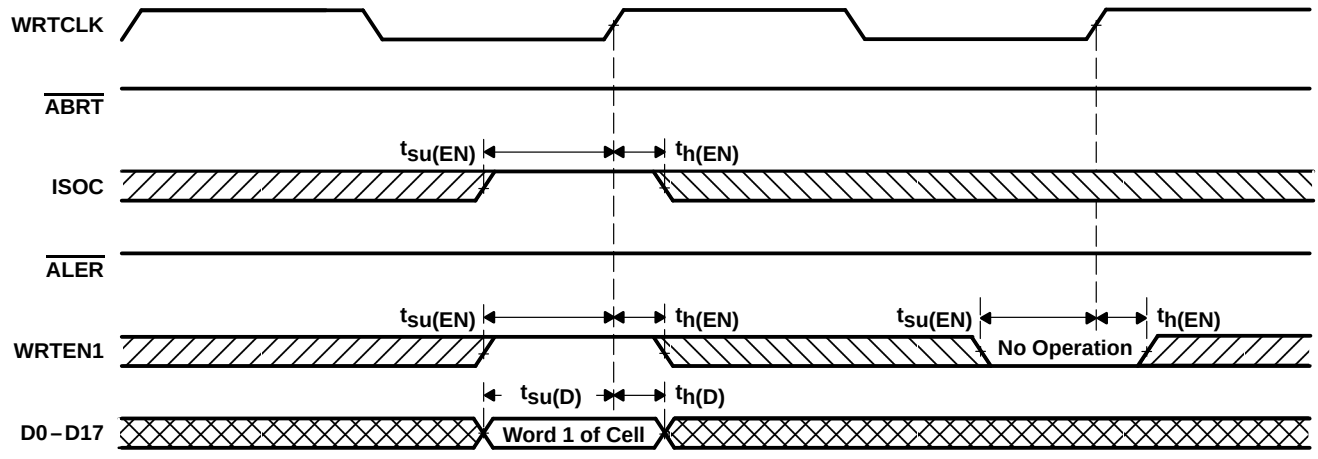
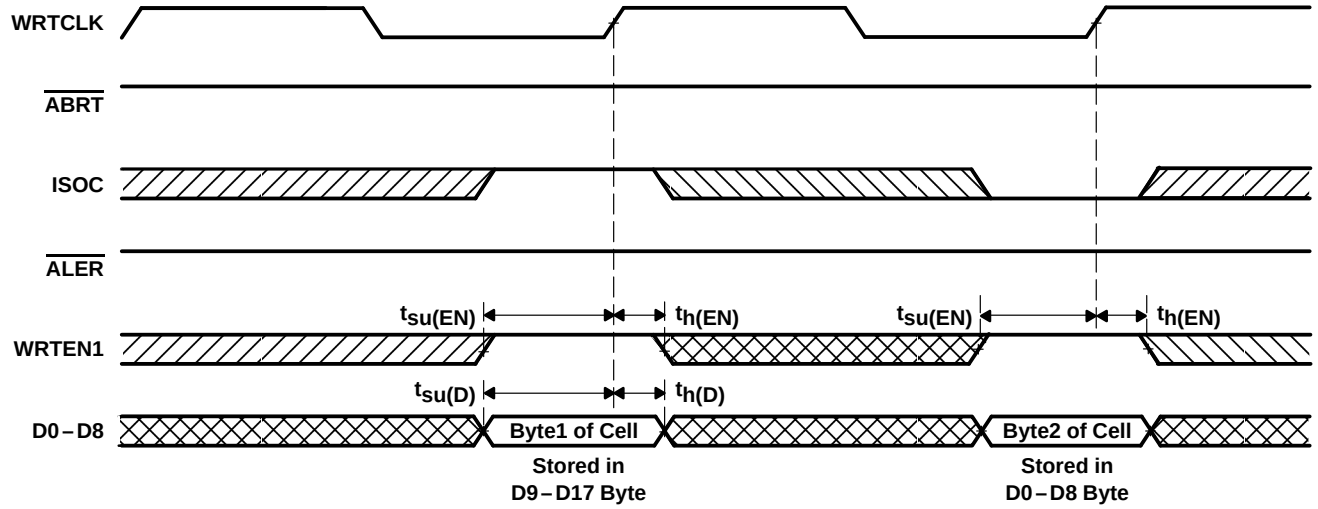


NOTES: A. DWRDY = H
B. Data is loaded to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
C. INSIZ bit of PORT register = 0

Figure 3. Writing Word-Length Data to Queue1



NOTES: A. DWRDY = H
B. Data is loaded to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
C. INSIZ bit of PORT register = 1; INBE bit of PORT register = 1.

Figure 4. Writing Byte Data to Queue1 in Big-Endian Configuration

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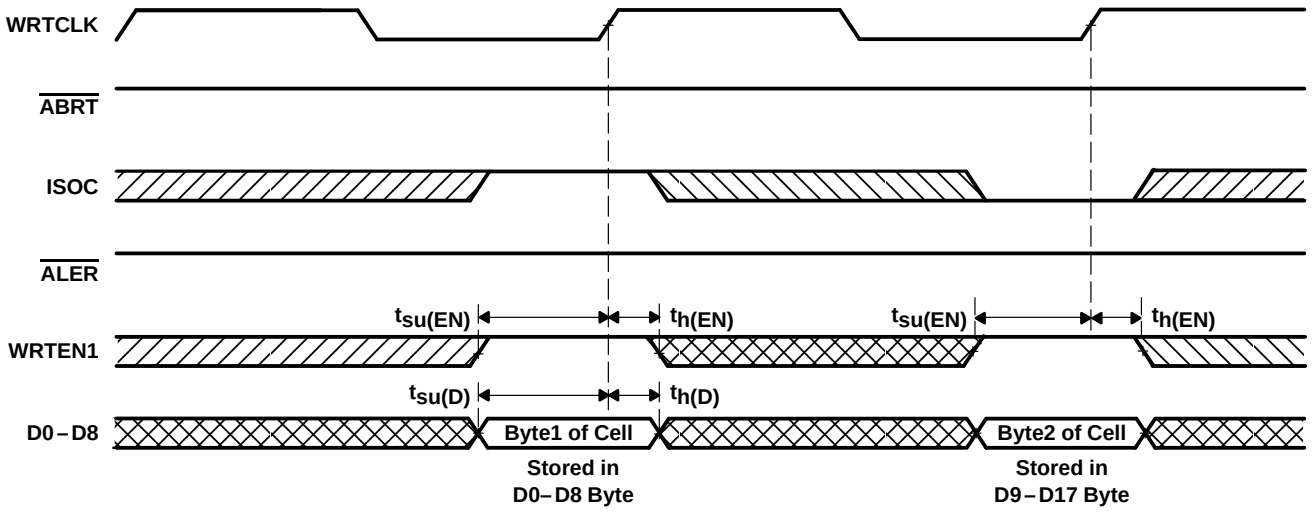
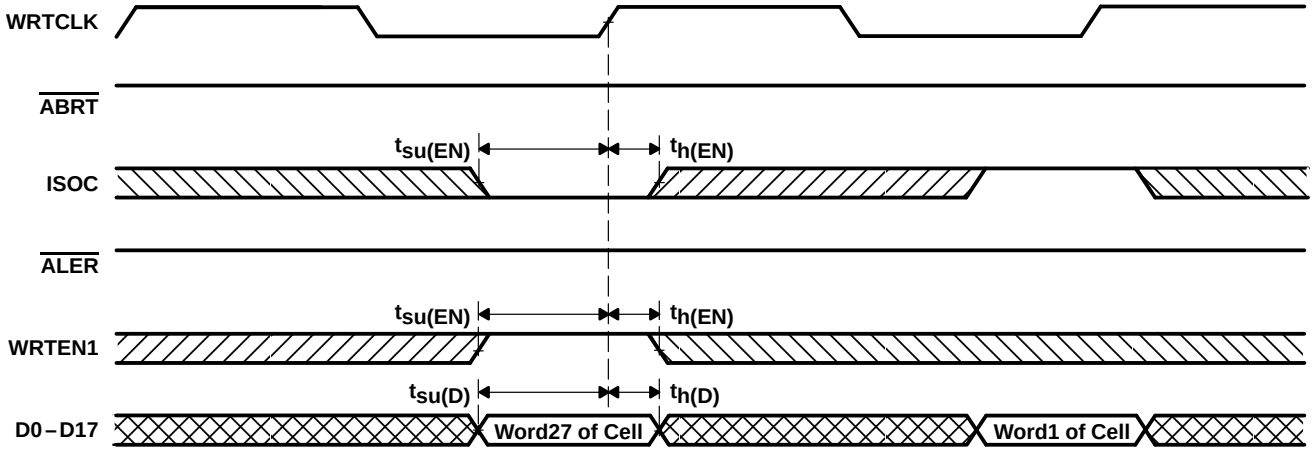


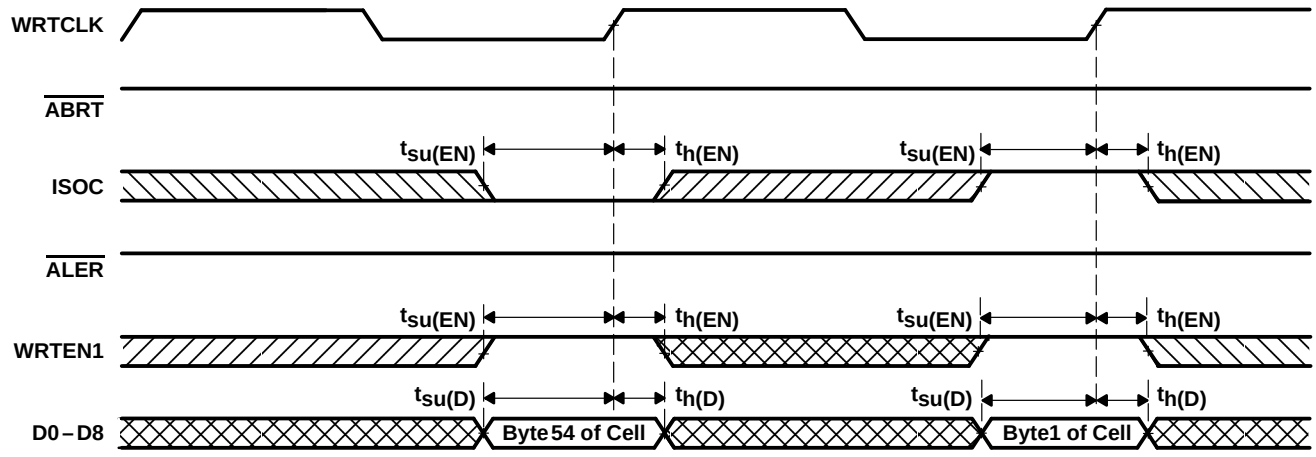
NOTES: A. DWRDY = H
B. Data is loaded to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
C. INSIZ bit of PORT register = 1; INBE bit of PORT register = 0.

Figure 5. Writing Byte Data to Queue1 in Little-Endian Configuration



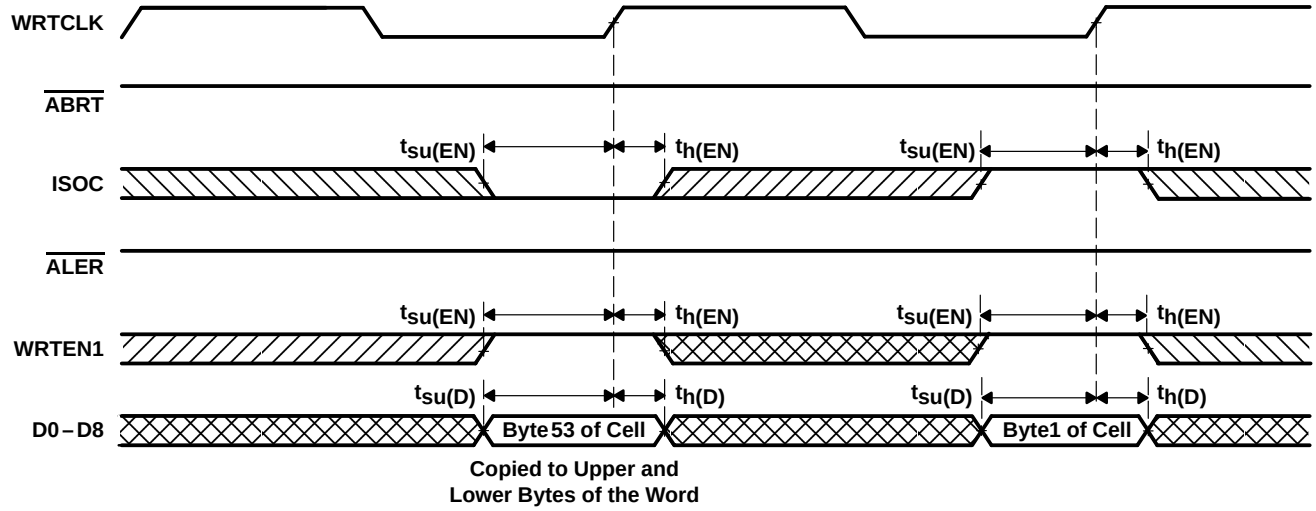
NOTES: A. CLSZ = 27 for the example
B. DWRDY = H
C. A cell is confirmed to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
D. INSIZ bit of PORT register = 0

Figure 6. Cell-Write Completion With 18-Bit Input



NOTES: A. CLSZ = 27 for the example
B. DWRDY = H
C. A cell is confirmed to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
D. INSIZ bit of PORT register = 1; INSTF bit of PORT register = 0.

Figure 7. Cell-Write-Completion Example With 9-Bit Input and No Byte Stuffing



NOTES: A. CLSZ = 27 for the example
B. DWRDY = H
C. A cell is confirmed to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
D. INSIZ bit of PORT register = 1; INSTF bit of PORT register = 1.

Figure 8. Cell-Write-Completion Example With 9-Bit Input and Byte Stuffing

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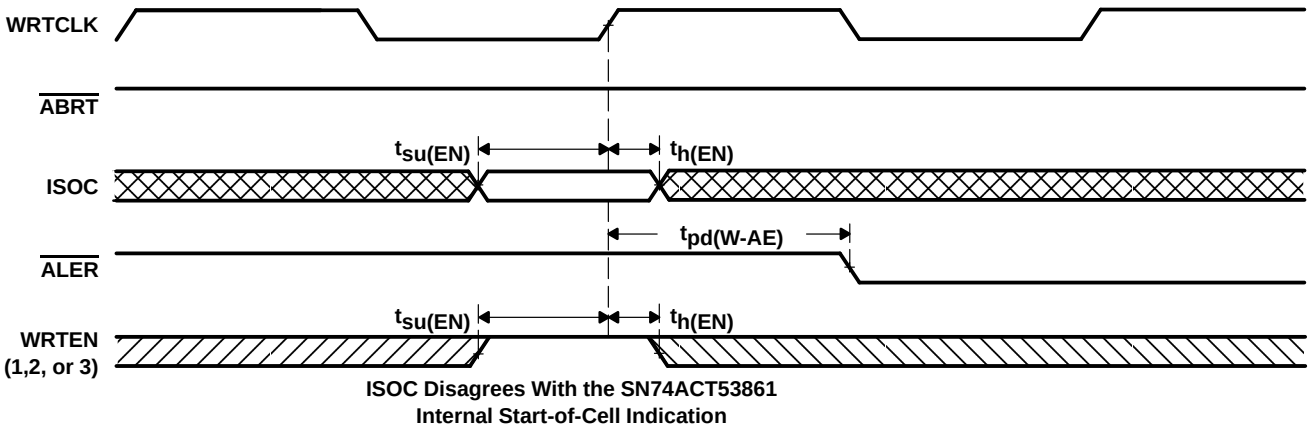
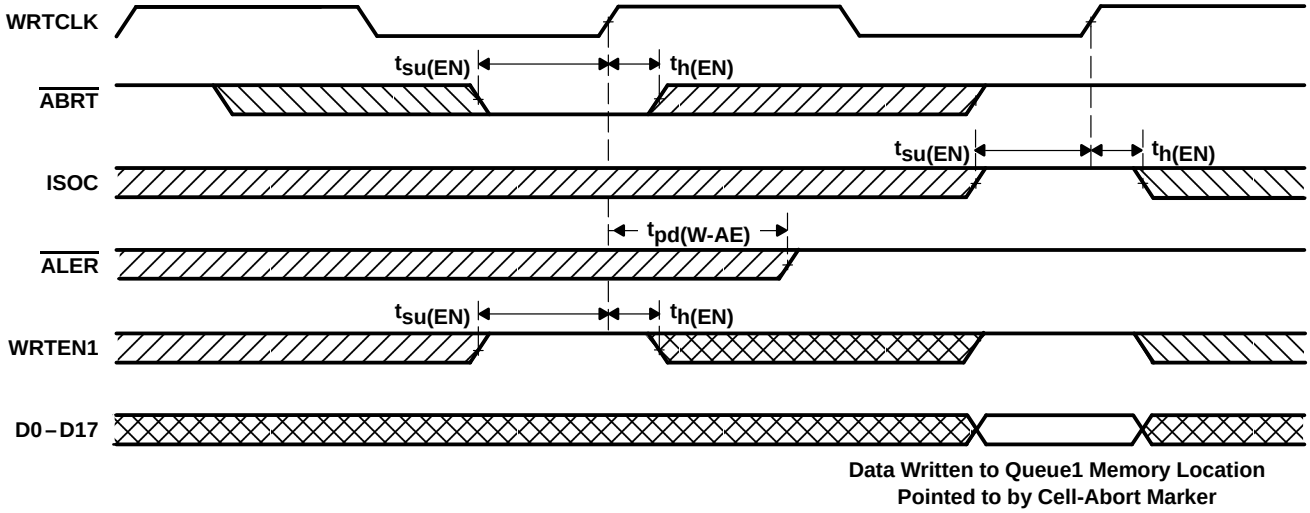


Figure 9. Setting $\overline{\text{ALER}}$ When ISOC Is Misaligned



NOTES: A. DWRDY = H
B. Data written since the last confirmation in Queue2 or Queue3 are aborted in the same manner when the corresponding WRTEN is active.

Figure 10. Aborting Data In Queue1 Written Since the Last Cell Completion

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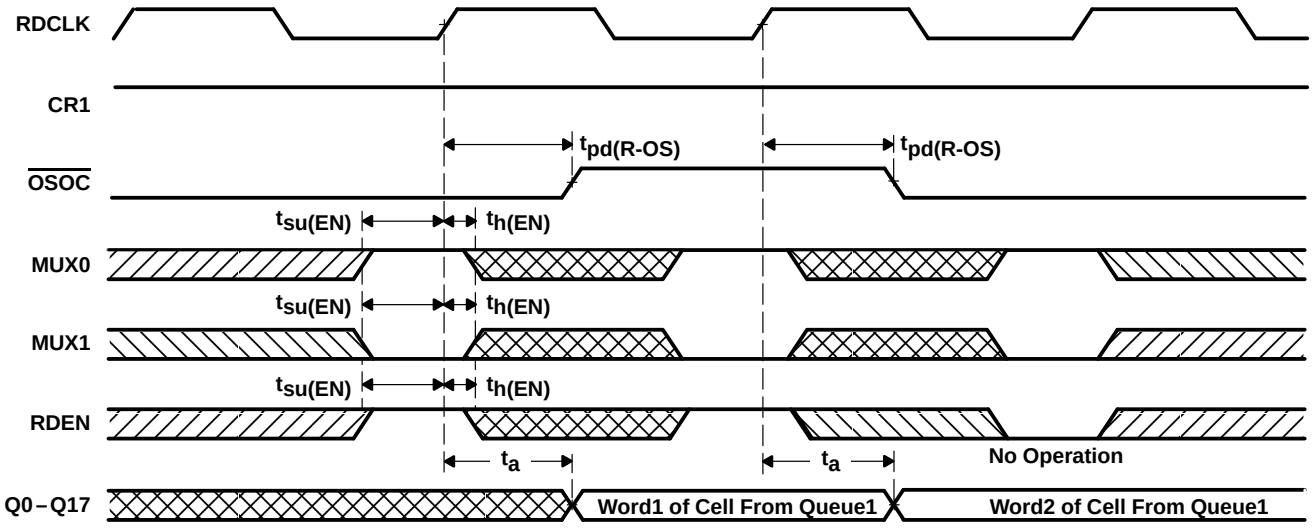
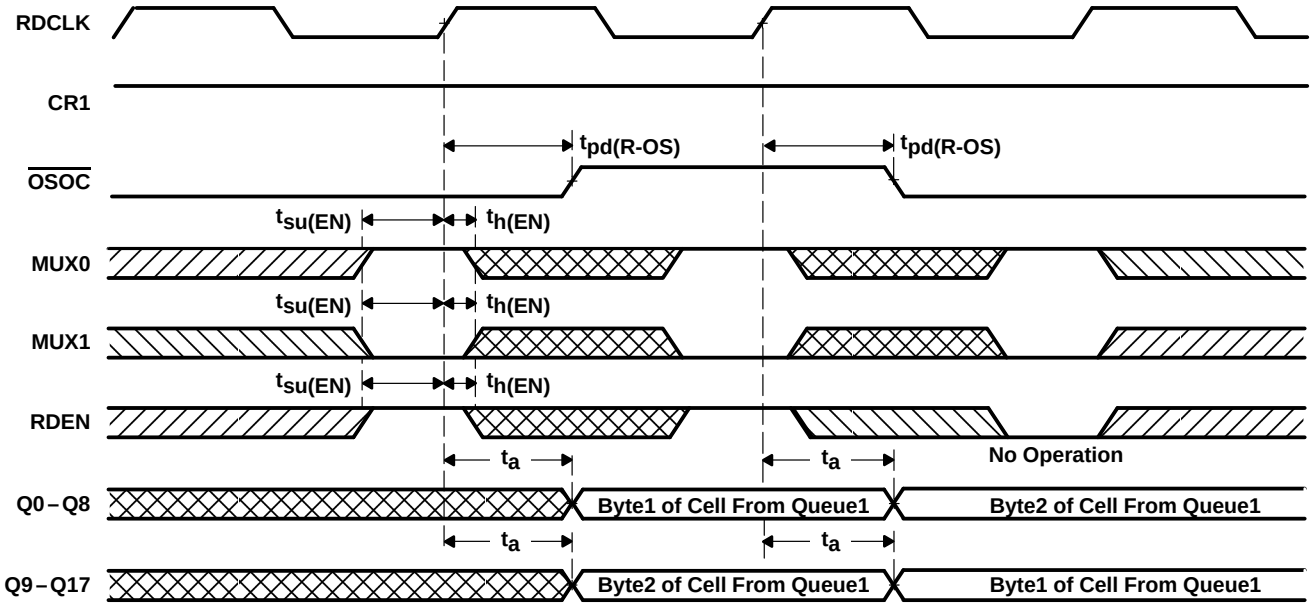


NOTES: A. OE = H
B. Data is read from Queue2 in the same manner when CR2 is high with MUX1 = H and MUX0 = L. Data is read from Queue3 in the same manner when CR3 is high with MUX1 = H and MUX0 = H.
C. OUTSIZ bit of PORT register = 0

Figure 11. Reading Word-Size Data From Queue1



NOTES: A. OE = H
B. Data is read from Queue2 in the same manner when CR2 is high with MUX1 = H and MUX0 = L. Data is read from Queue3 in the same manner when CR3 is high with MUX1 = H and MUX0 = H.
C. OUTSIZ bit of PORT register = 1

Figure 12. Reading Byte-Size Data From Queue1

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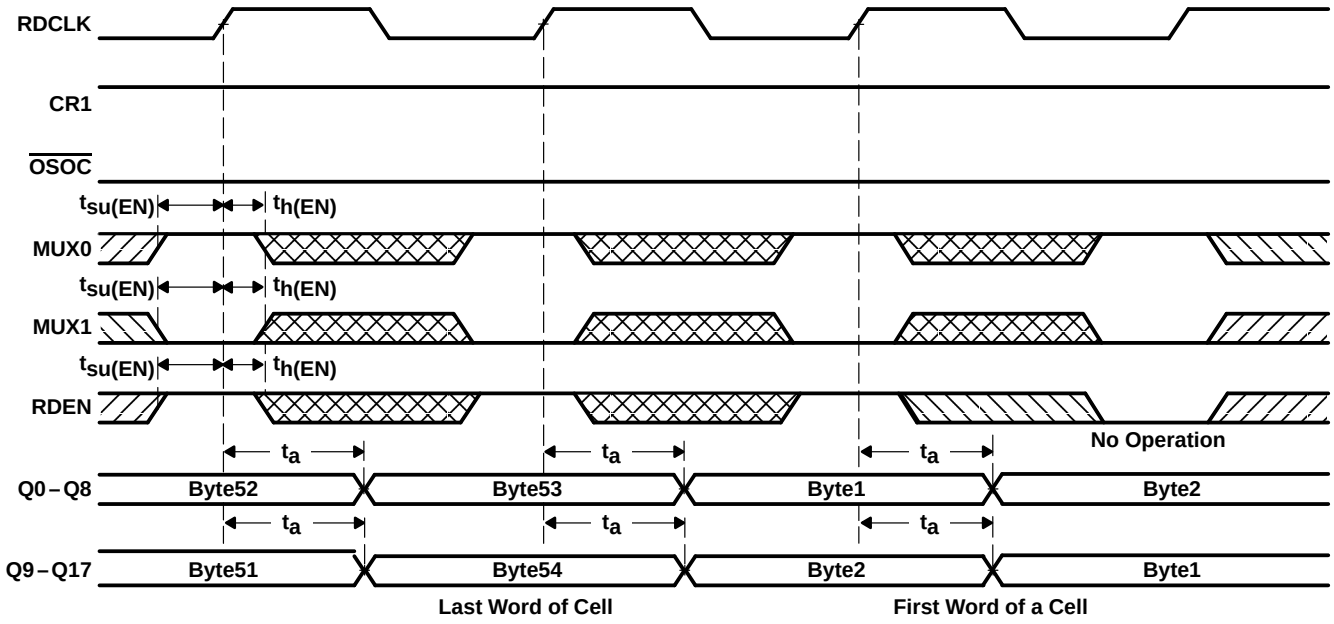
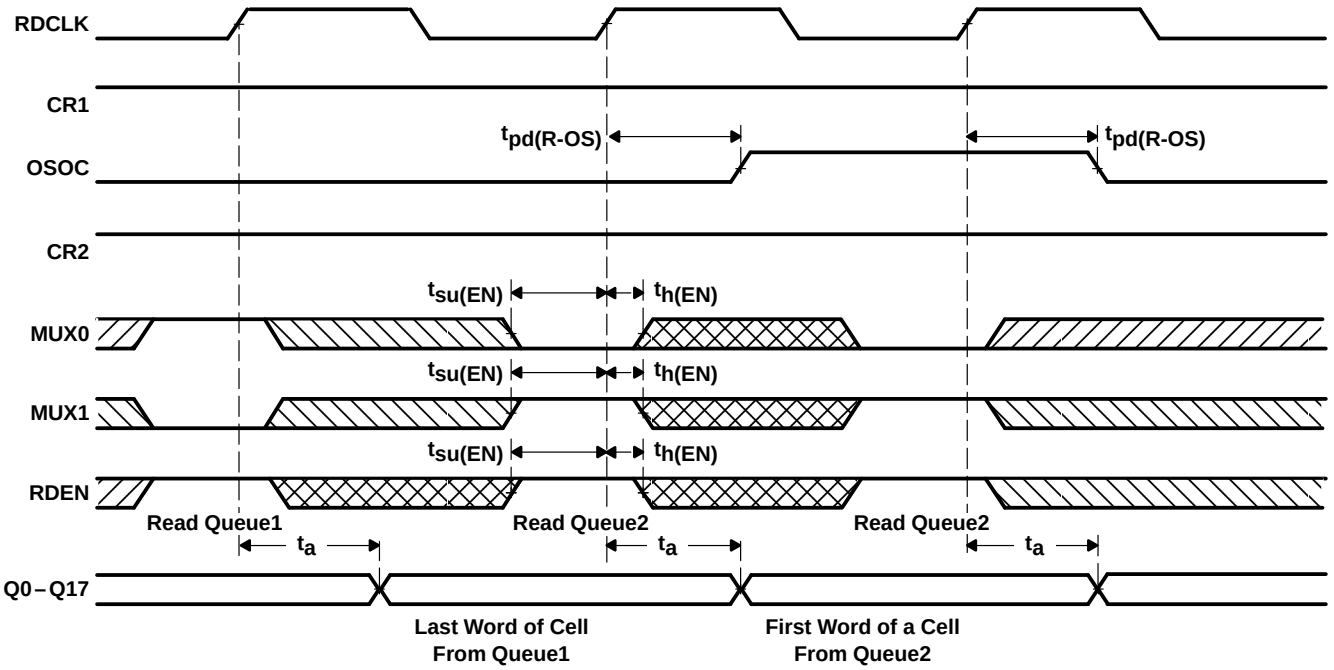


NOTES: A. CLSZ = 27 for the example
B. OE = H
C. Data is read from Queue2 in the same manner when CR2 is high with MUX1 = H and MUX0 = L. Data is read from Queue3 in the same manner when CR3 is high with MUX1 = H and MUX0 = H.
D. OUTSIZ bit of PORT register = 1; OUTSTF bit of PORT register = 1.

Figure 13. Reading Byte-Size Data With Byte Destuffing



NOTES: A. OE = H
B. If a read from Queue2 is disabled by CR2 low or RDEN low during the cycle the output switch occurs, the previous data held in the Queue2 output register is output.
C. OUTSIZ bit of PORT register = 0

Figure 14. Example of Switching Queues on the Output

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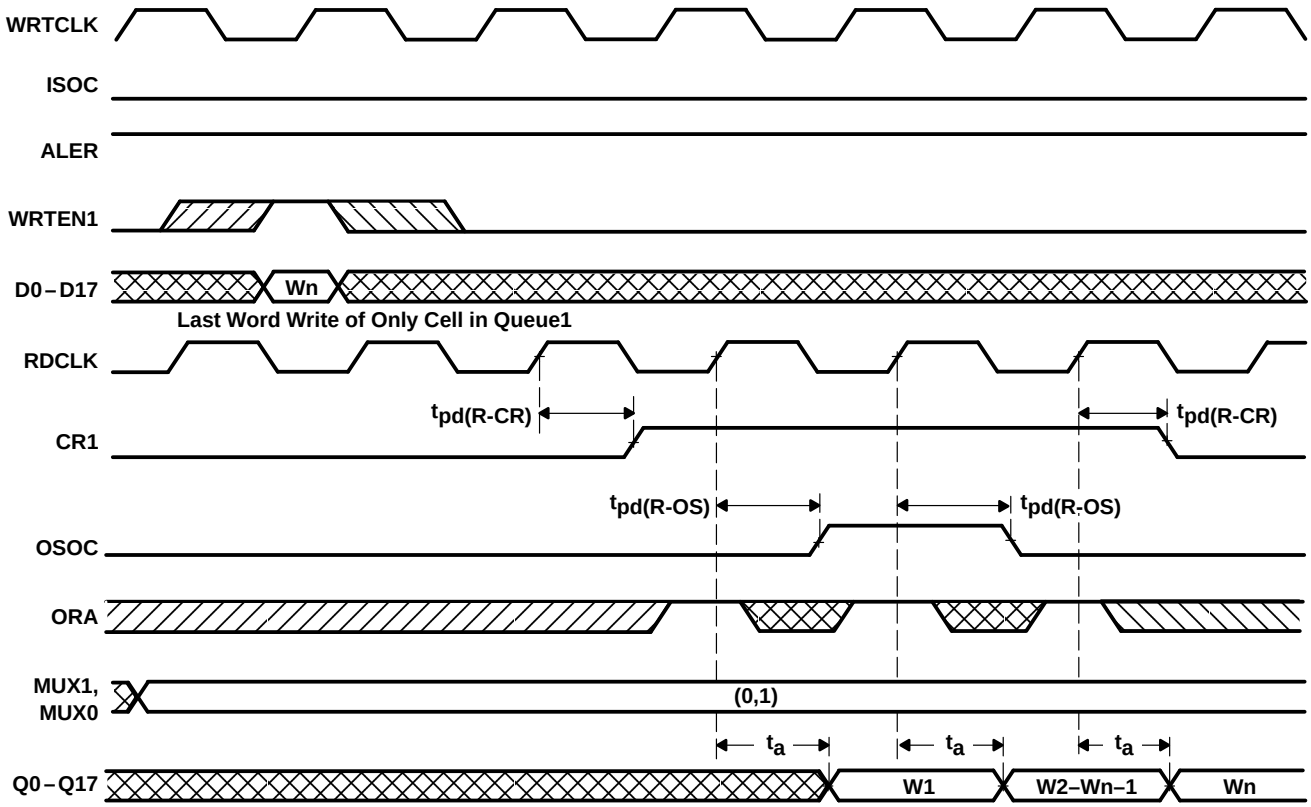

NOTES: A. Outputs enabled (OE = H); word bus size
B. When byte size output bus is used:
– If OUTSTF bit of PORT register = 1, CR1 set low by first byte read of Wn.
– If OUTSTF bit of PORT register = 0, CR1 set low by last byte read of Wn.

Figure 15. CR1 Timing Example

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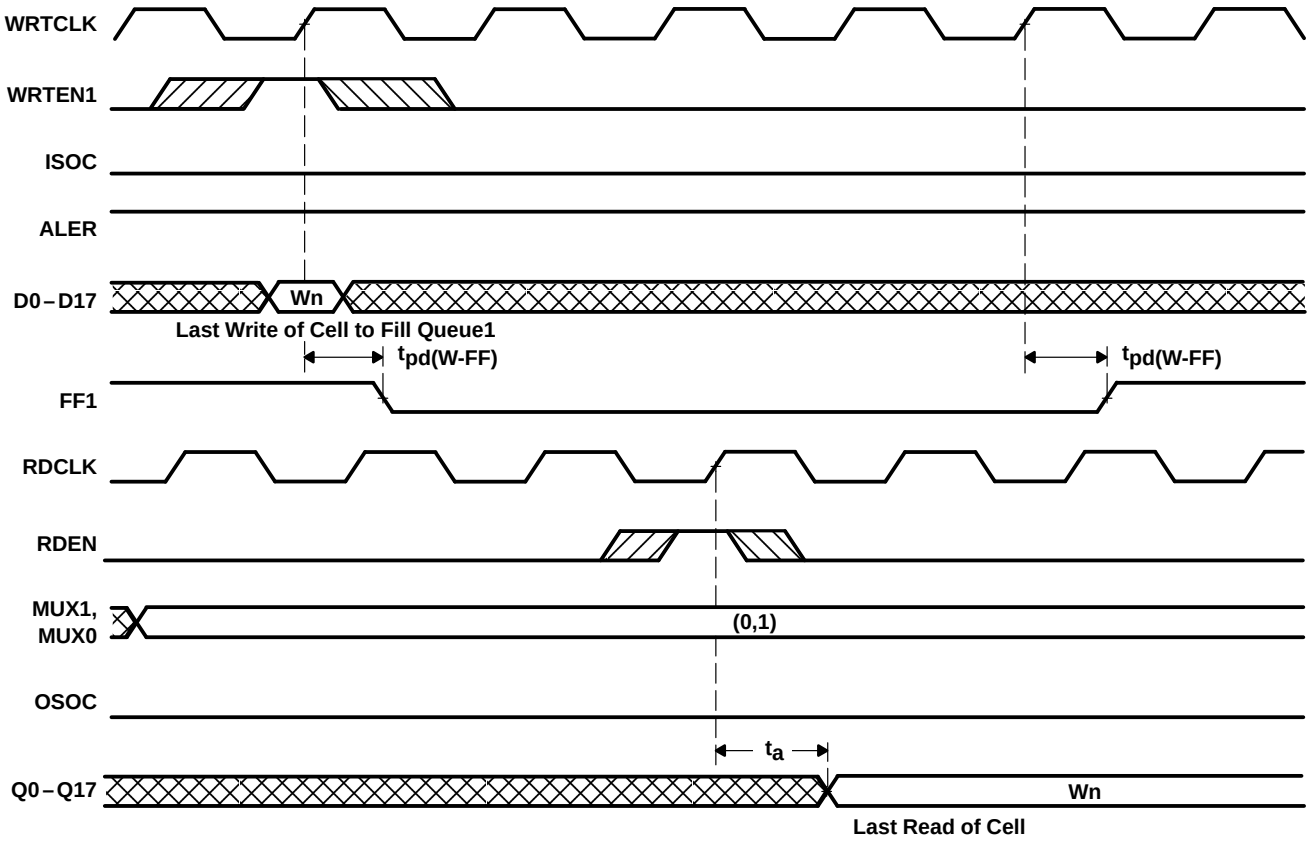

NOTES: A. Outputs enabled (OE = H); word bus size
B. When byte size output bus is used:
– If OUTSTF bit of PORT register = 1, FF1 set low by first byte read of Wn.
– If OUTSTF bit of PORT register = 0, FF1 set low by last byte read of Wn.

Figure 16. $\overline{\text{FF1}}$ Timing Example

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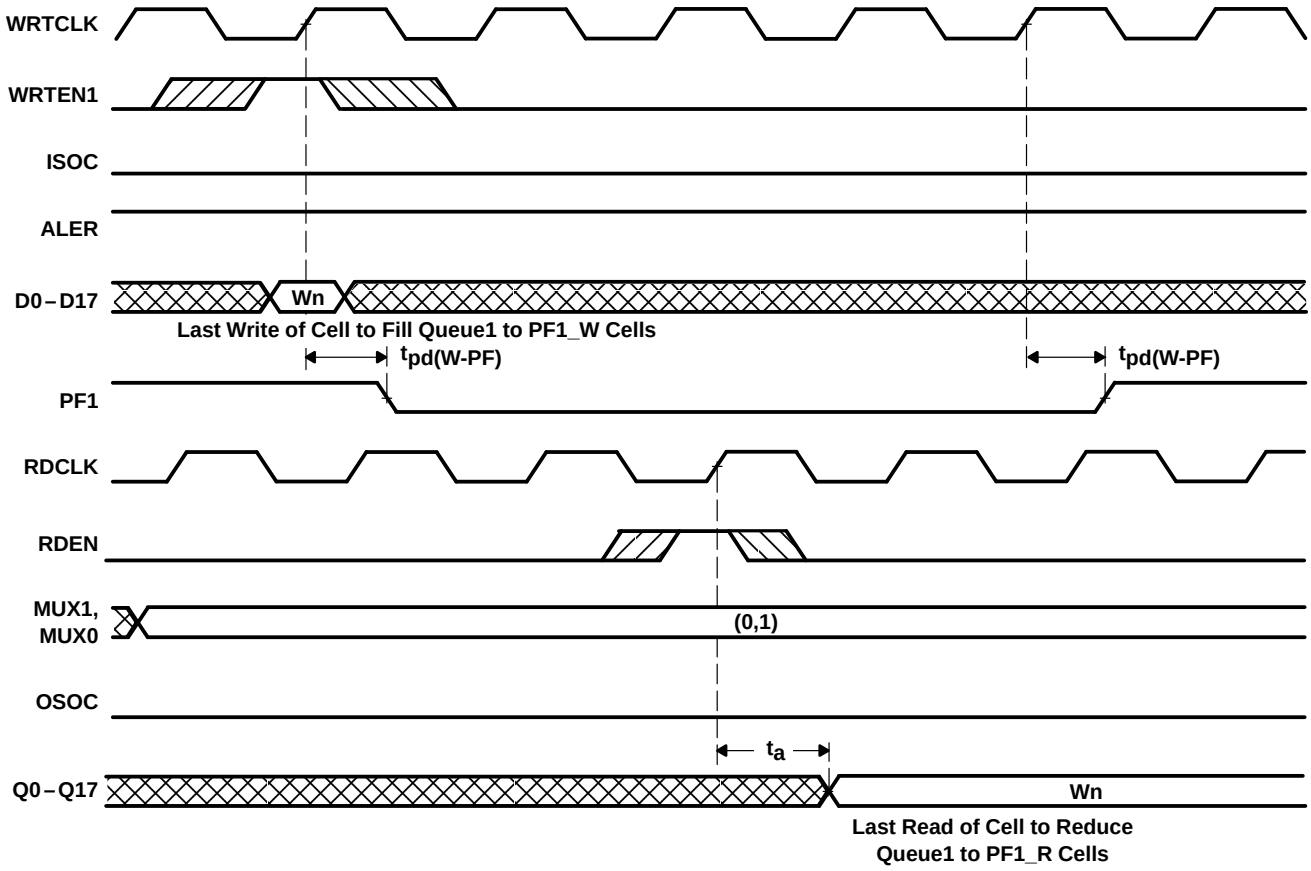

NOTES: A. Outputs enabled (OE = H); word bus size
B. When byte size output bus is used:
– If OUTSTF bit of PORT register = 1, PF1 set low by first byte read of Wn.
– If OUTSTF bit of PORT register = 0, PF1 set low by last byte read of Wn.

Figure 17. PF1 Timing Example

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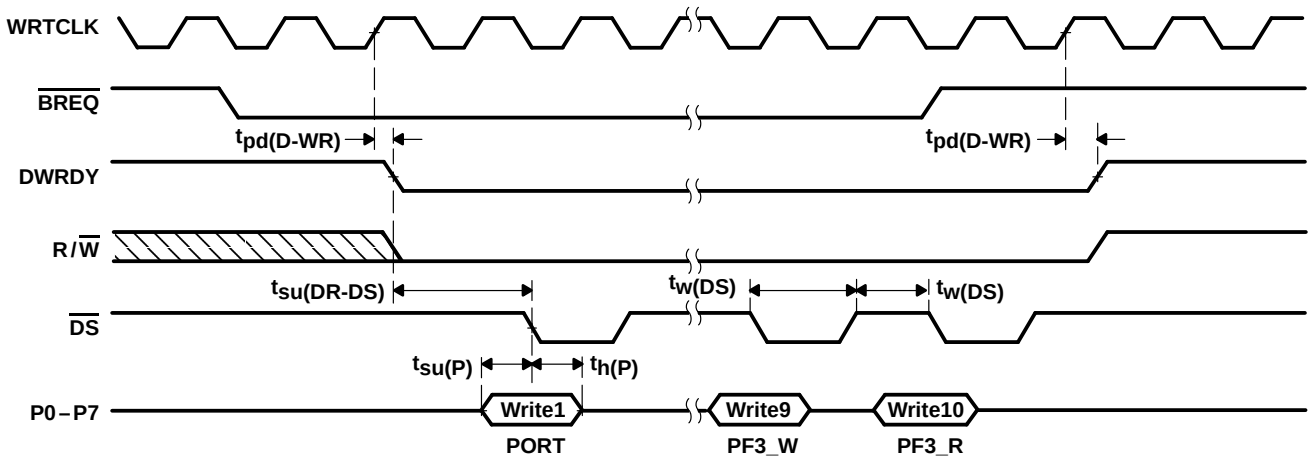


Figure 18. Writing to the Programming Registers

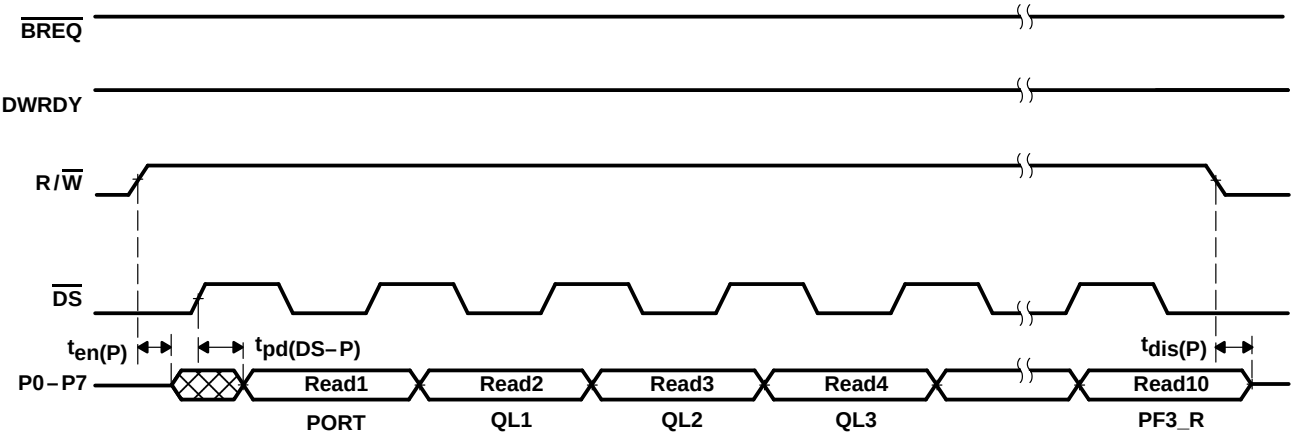


Figure 19. Reading From the Programming Registers

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±400 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –4 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}	V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	µA
ΔI_{CC}§	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz			4		pF
C_o	V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 2 through 19)

		MIN	MAX	UNIT
f_{clock}	Clock frequency, WRTCLK or RDCLK		50	MHz
t_c	Clock cycle time, WRTCLK or RDCLK	20		ns
$t_{w(CLKH)}$	Pulse duration, WRTCLK and RDCLK high	7		ns
$t_{w(CLKL)}$	Pulse duration, WRTCLK and RDCLK low	7		ns
$t_{w(DS)}$	Pulse duration, $\overline{DS}$ high or low	15		ns
$t_{su(D)}$	Setup time, D0–D17 before WRTCLK↑	5		ns
$t_{su(EN)}$	Setup time, ISOC, $\overline{ABRT}$, WRTEN1, WRTEN2, and WRTEN3 before WRTCLK↑; RDEN, MUX0, and MUX1 before RDCLK↑	5		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before WRTCLK↑ or RDCLK↑†	7		ns
$t_{su(RS2)}$	Setup time, $\overline{RST}$ high before first data write	20		ns
$t_{su(R–DS)}$	Setup time, R/$\overline{W}$ before $\overline{DS}$↓	8		ns
$t_{su(DR–DS)}$	Setup time, DWRDY before $\overline{DS}$↓	8		ns
$t_{su(P)}$	Setup time, P0–P7 before $\overline{DS}$↓	8		ns
$t_{h(D)}$	Hold time, D0–D17 after WRTCLK↑	0		ns
$t_{h(EN)}$	Hold time, ISOC, $\overline{ABRT}$, WRTEN1, WRTEN2, and WRTEN3 after WRTCLK↑; RDEN, MUX0, and MUX1 after RDCLK↑	0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after WRTCLK↑ or RDCLK↑†	7		ns
$t_{h(R–DS)}$	Hold time, R/$\overline{W}$ after $\overline{DS}$↓	1		ns
$t_{h(P)}$	Hold time, P0–P7 after $\overline{DS}$↓	1		ns

† Requirement to count the clock edge as one of at least four needed to reset a FIFO

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 20 and 21)

PARAMETER		MIN	MAX	UNIT
t_a	Access time, RDCLK↑ to Q0–Q17		11	ns
$t_{pd(R-CR)}$	Propagation delay time, RDCLK↑ to CR1, CR2, or CR3		10	ns
$t_{pd(R-OS)}$	Propagation delay time, RDCLK↑ to OSOC		10	ns
$t_{pd(W-AE)}$	Propagation delay time, WRTCLK↑ to $\overline{ALER}$		10	ns
$t_{pd(W-PF)}$	Propagation delay time, WRTCLK↑ to PF1, PF2, or PF3		10	ns
$t_{pd(W-FF)}$	Propagation delay time, WRTCLK↑ to $\overline{FF1}$, $\overline{FF2}$, or $\overline{FF3}$		10	ns
$t_{pd(W-WR)}$	Propagation delay time, WRTCLK↑ to DWRDY		10	ns
$t_{pd(DS–P)}$	Propagation delay time, $\overline{DS}$↑ to P0–P7		20	ns
$t_{en(Q)}$	Enable time, OE to Q0–Q17 active	1		ns
$t_{dis(Q)}$	Disable time, OE to Q0–Q17 at high impedance		9	ns
$t_{en(P)}$	Enable time, $\overline{POE}$ and R/$\overline{W}$ to P0–P7 active	1		ns
$t_{dis(P)}$	Disable time, $\overline{POE}$ and R/$\overline{W}$ to P0–P7 at high impedance		9	ns

PARAMETER MEASUREMENT INFORMATION

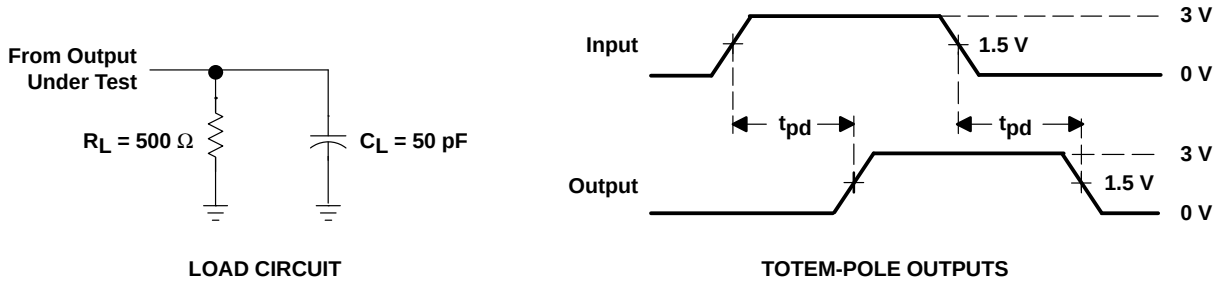
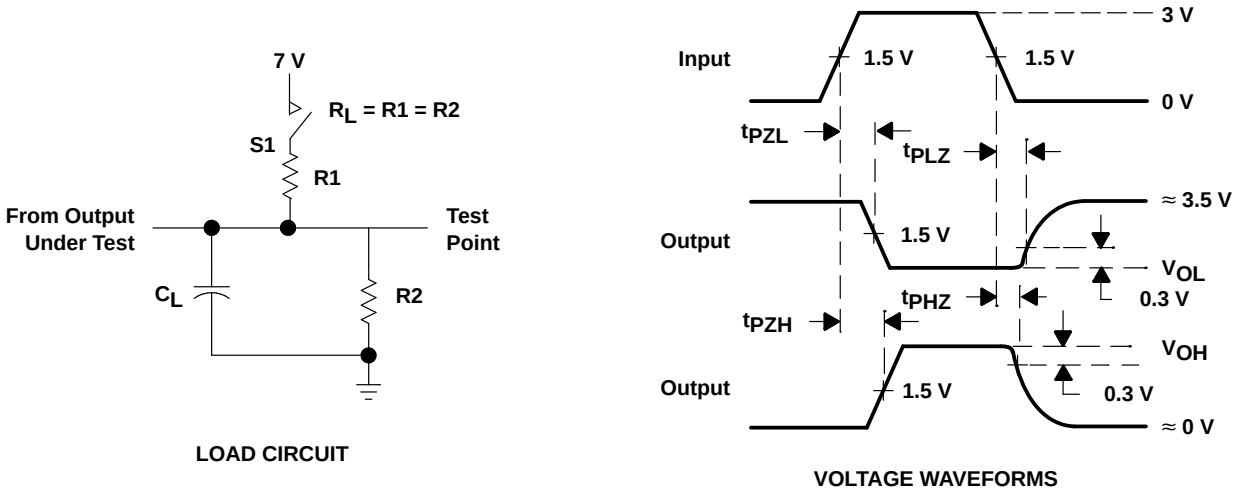


Figure 20. Standard CMOS Outputs



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 21. 3-State Outputs

PRODUCT PREVIEW

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