

SN74ALVC7804, SN74ALVC7806, SN74ALVC7814
512 × 18, 256 × 18, 64 × 18
LOW-POWERED FIRST-IN, FIRST-OUT MEMORIES
 SCAS437C – JUNE 1994 – REVISED FEBRUARY 1996

- Operate at 3-V to 3.6-V V_{CC}
- Load Clock and Unload Clock Can Be Asynchronous or Coincident
- Low-Power Advanced CMOS Technology
- Full, Empty, and Half-Full Flags
- Programmable Almost-Full/Almost-Empty Flag
- Fast Access Times of 18 ns With a 50-pF Load and All Data Outputs Switching Simultaneously
- Data Rates From 0 to 40 MHz
- 3-State Outputs
- Pin Compatible With SN74ACT7804, SN74ACT7806, and SN74ACT7814
- Available in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing

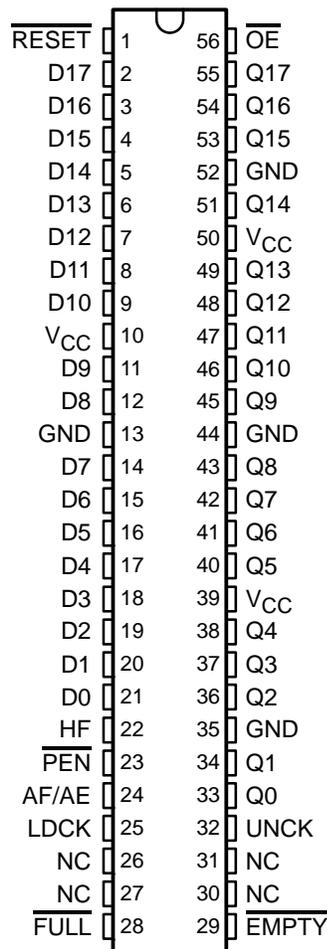
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALVC7804, SN74ALVC7806, and SN74ALVC7814 are 18-bit FIFOs with high speed and fast access times. Data is processed at rates up to 40 MHz with access times of 18 ns in a bit-parallel format. These memories are designed for 3-V to 3.6-V V_{CC} operation.

Data is written into memory on a low-to-high transition of the load clock (LDCK) and is read out on a low-to-high transition of the unload clock (UNCK). The memory is full when the number of words clocked in exceeds the number of words clocked out by 512. When the memory is full, LDCK has no effect on the data residing in memory. When the memory is empty, UNCK has no effect.

Status of the FIFO memory is monitored by the full (\overline{FULL}), empty (\overline{EMPTY}), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The \overline{FULL} output is low when the memory is full and high when the memory is not full. The \overline{EMPTY} output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 256 or more words and low when it contains 255 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable (\overline{PEN}) is low. The AF/AE flag is high when the FIFO contains X or fewer words or 512 – Y or more words. The AF/AE flag is low when the FIFO contains between X + 1 and 511 – Y words.

DL PACKAGE
(TOP VIEW)



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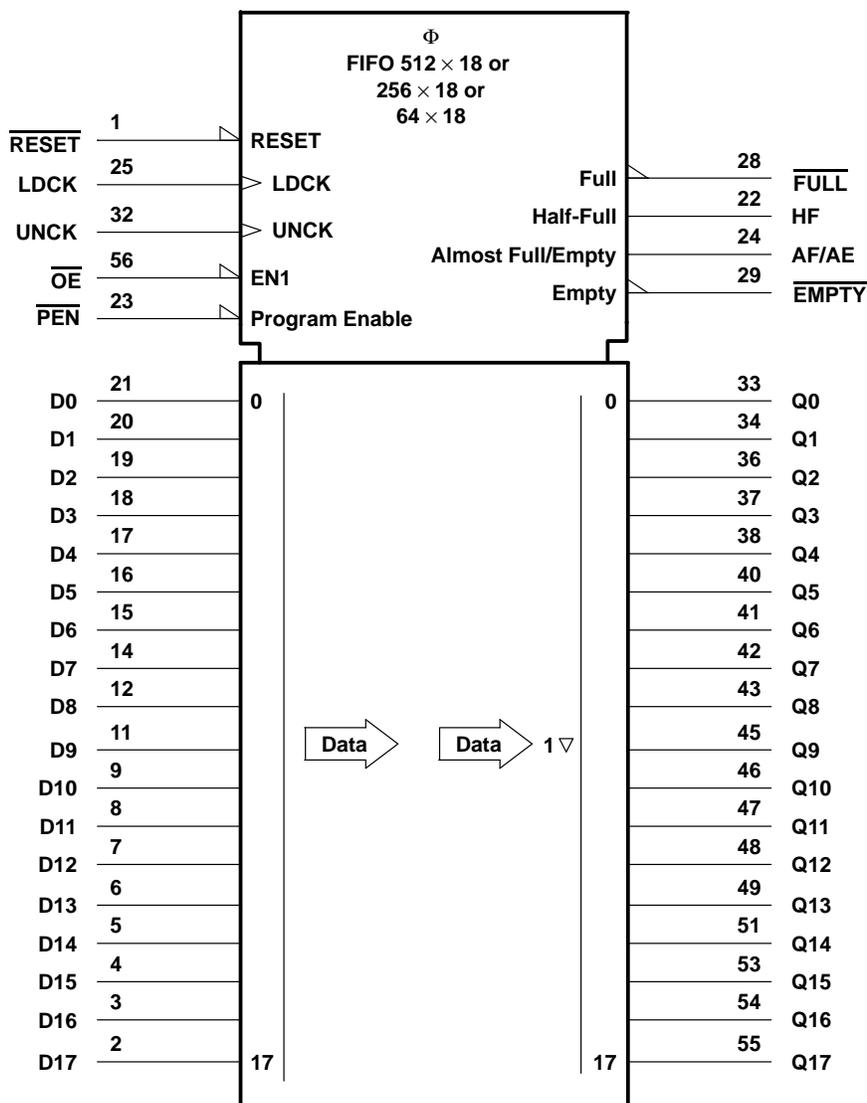
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description (continued)

A low level on the reset ($\overline{\text{RESET}}$) resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset on power up. The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The data outputs are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) is high.

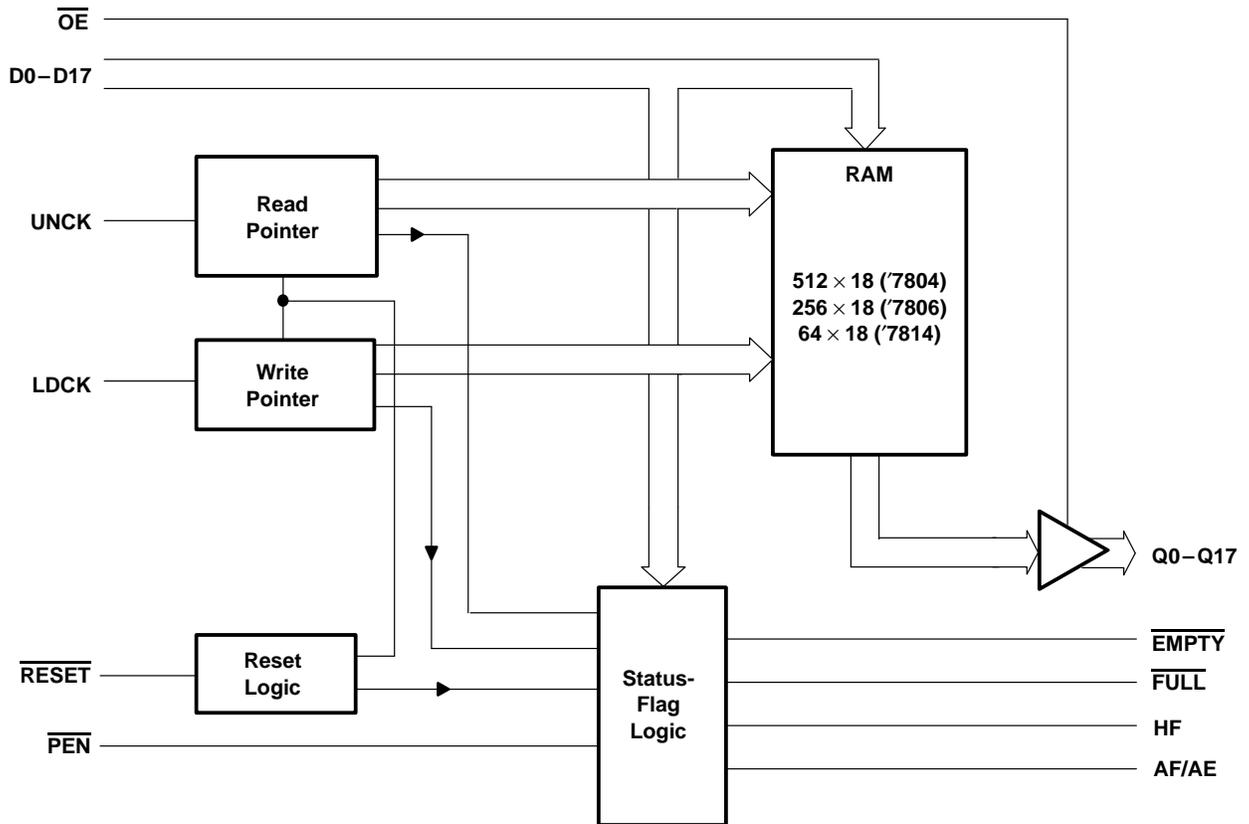
The SN74ALVC7804, SN74ALVC7806, and SN74ALVC7814 are characterized for operation from 0°C to 70°C.

logic symbol†



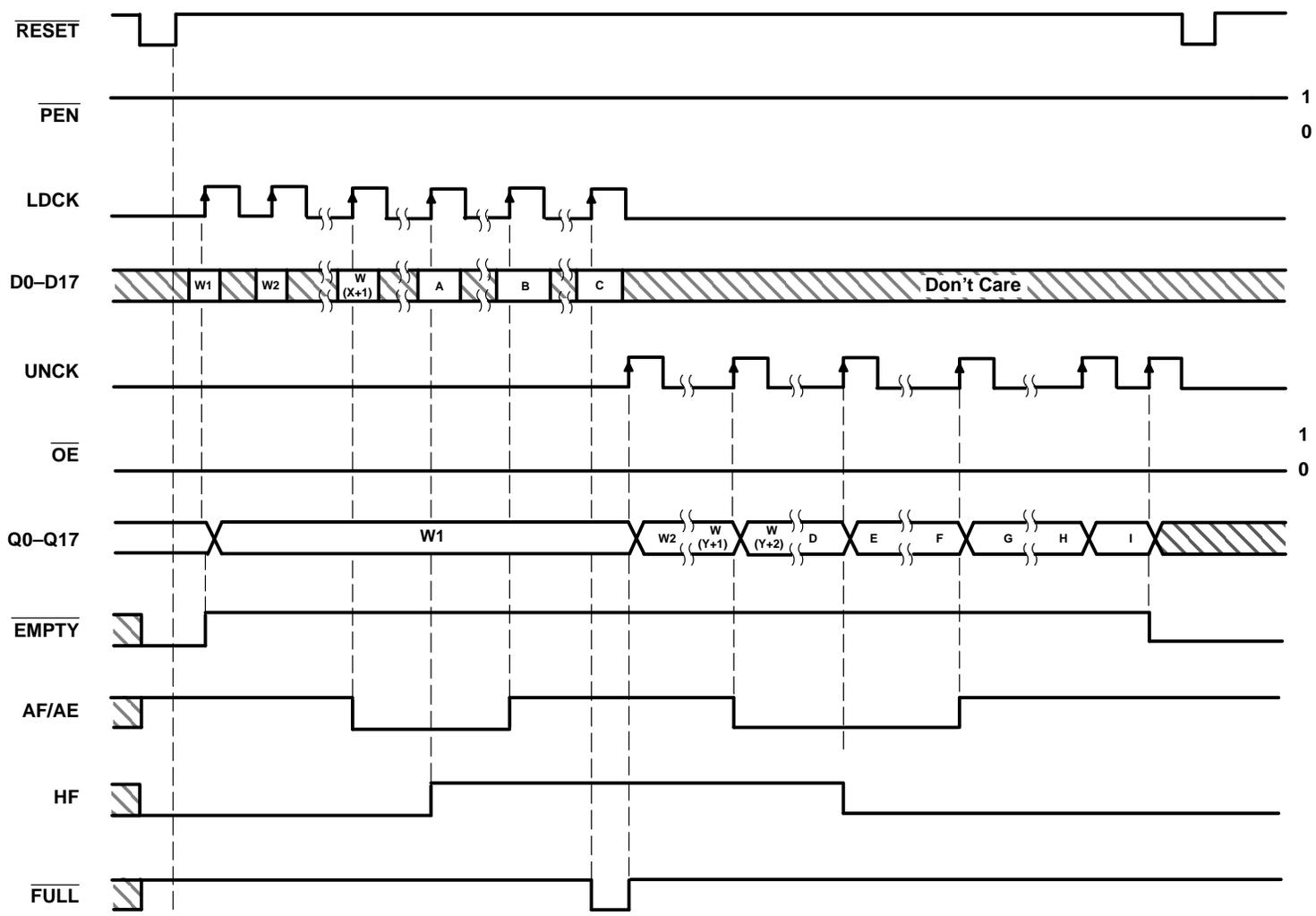
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost full/almost empty flag. Depth-offset values can be programmed for this flag or the default value of 64 can be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or fewer words or 512 – Y or more words. AF/AE is high after reset.
D0–D17	2–9, 11–12, 14–21	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.



Define the AF/AE Flag Using the Default Value of X and Y

Figure 1. Write, Read, and Flag Timing Reference

DATA WORD NUMBERS FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD								
	A	B	C	D	E	F	G	H	I
SN74ALVC7814	W32	W(64–Y)	W64	W33	W34	W(64–X)	W(65–X)	W64	W64
SN74ALVC7806	W128	W(256–Y)	W256	W129	W130	W(256–X)	W(257–X)	W255	W256
SN74ALVC7804	W256	W(512–Y)	W512	W257	W258	W(512–X)	W(513–X)	W511	W512

Figure 1. Write, Read, and Flag Timing Reference (Continued)

offset values for AF/AE

The almost-full/almost-empty (AF/AE) flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or fewer words or 512 – Y or more words.

To program the offset values, \overline{PEN} can be brought low after reset. On the following low-to-high transition of LDCK, the binary value on D0–D7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding \overline{PEN} low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 255 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 64, \overline{PEN} must be held high.

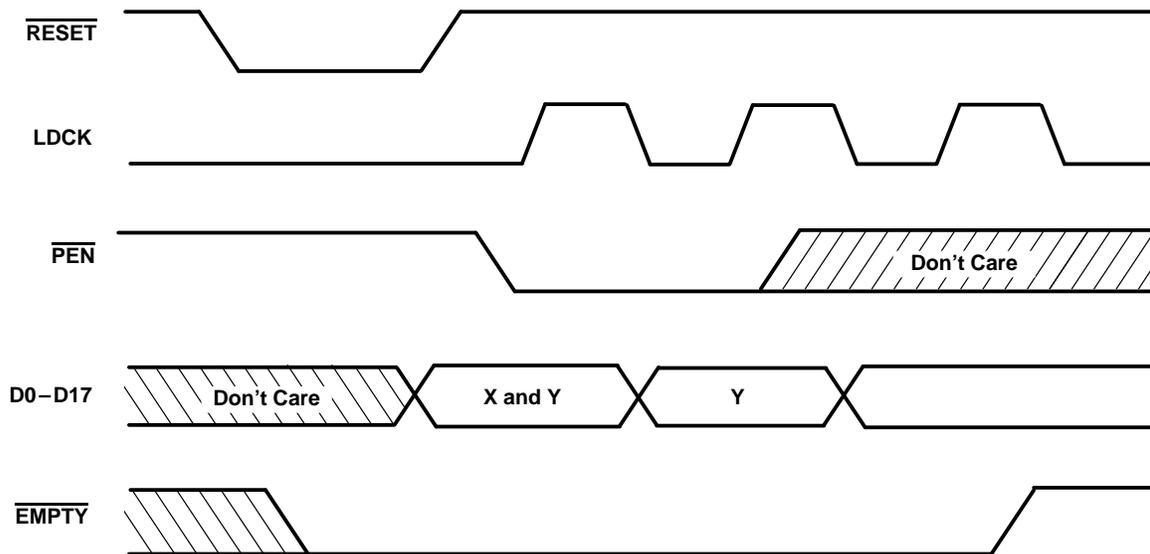


Figure 2. Programming X and Y Separately

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Voltage applied to a disabled 3-state output	3.6 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions

		SN74ALVC7804-25	SN74ALVC7804-40	UNIT		
		SN74ALVC7806-25	SN74ALVC7806-40			
		SN74ALVC7814-25	SN74ALVC7814-40			
		$V_{CC} = 3.3$ V ± 0.3 V				
		MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	2		2	V	
V_{IL}	Low-level input voltage	0.8		0.8	V	
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current, Q outputs, flags	$V_{CC} = 3$ V		–8	–8	mA
I_{OL}	Low-level output current, Q outputs, flags	$V_{CC} = 3$ V		16	16	mA
f_{clock}	Clock frequency	40		25	MHz	
t_w	Pulse duration	D0–D17 high or low		8	12	ns
		LDCK high or low		8	12	
		UNCK high or low		8	12	
		\overline{PEN} low		8	12	
		RESET low		10	12	
t_{su}	Setup time	D0–D17 before LDCK↑		5	5	ns
		LDCK inactive before RESET high		6	6	
		\overline{PEN} before LDCK↑		8	8	
t_h	Hold time	D0–D17 after LDCK↑		0	0	ns
		\overline{PEN} high after LDCK low		0	0	
		\overline{PEN} low after LDCK↑		3	3	
		LDCK inactive after RESET high		6	6	
T_A	Operating free-air temperature	0	70	0	70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION [†]		MIN	TYP [‡]	MAX	UNIT
V _{OH}	Flags, Q outputs	V _{CC} = MIN to MAX,	I _{OH} = – 100 μA	V _{CC} – 0.2		V	
		V _{CC} = 3 V,	I _{OH} = – 8 mA	2.4			
V _{OL}	Flags, Q outputs	V _{CC} = MIN to MAX,	I _{OL} = 100 μA	0.2		V	
	Flags	V _{CC} = 3 V,	I _{OL} = 8 mA	0.4			
	Q outputs	V _{CC} = 3 V,	I _{OL} = 16 mA	0.55			
I _I		V _{CC} = 3.6 V,	V _I = V _{CC} or GND	±5		μA	
I _{OZ}		V _{CC} = 3.6 V,	V _O = V _{CC} or GND	±10		μA	
I _{CC}		V _{CC} = 3.6 V,	V _I = V _{CC} or GND and I _O = 0	40		μA	
ΔI _{CC} [§]		V _{CC} = 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,	500		μA	
C _i		V _{CC} = 3.3 V,	V _I = V _{CC} or GND	3		pF	
C _o		V _{CC} = 3.3 V,	V _O = V _{CC} or GND	6		pF	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[§] This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ALVC7804-25 SN74ALVC7806-25 SN74ALVC7814-25		SN74ALVC7804-40 SN74ALVC7806-40 SN74ALVC7814-40		UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}	LDCK or UNCK		40		25		MHz
t _{pd}	LDCK↑	Any Q	9	22	9	24	ns
t _{pd}	UNCK↑		6	18	6	20	
t _{PLH}	LDCK↑	EMPTY	6	17	6	19	ns
t _{PHL}	UNCK↑		6	17	6	19	
t _{PHL}	RESET low		4	18	4	20	
t _{PHL}	LDCK↑	FULL	6	17	6	19	ns
t _{PLH}	UNCK↑		6	17	6	19	
t _{PLH}	RESET low		4	20	4	22	
t _{pd}	LDCK↑	AF/AE	7	20	7	22	ns
t _{pd}	UNCK↑		7	20	7	22	
t _{PLH}	RESET low		2	12	2	14	
t _{PLH}	LDCK↑	HF	5	20	5	22	ns
t _{PHL}	UNCK↑		7	20	7	22	
t _{PHL}	RESET low		3	14	3	16	
t _{en}	OE	Any Q	2	10	2	11	ns
t _{dis}			2	11	2	12	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled C _L = 50 pF, f = 5 MHz	53	pF



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APPLICATION INFORMATION

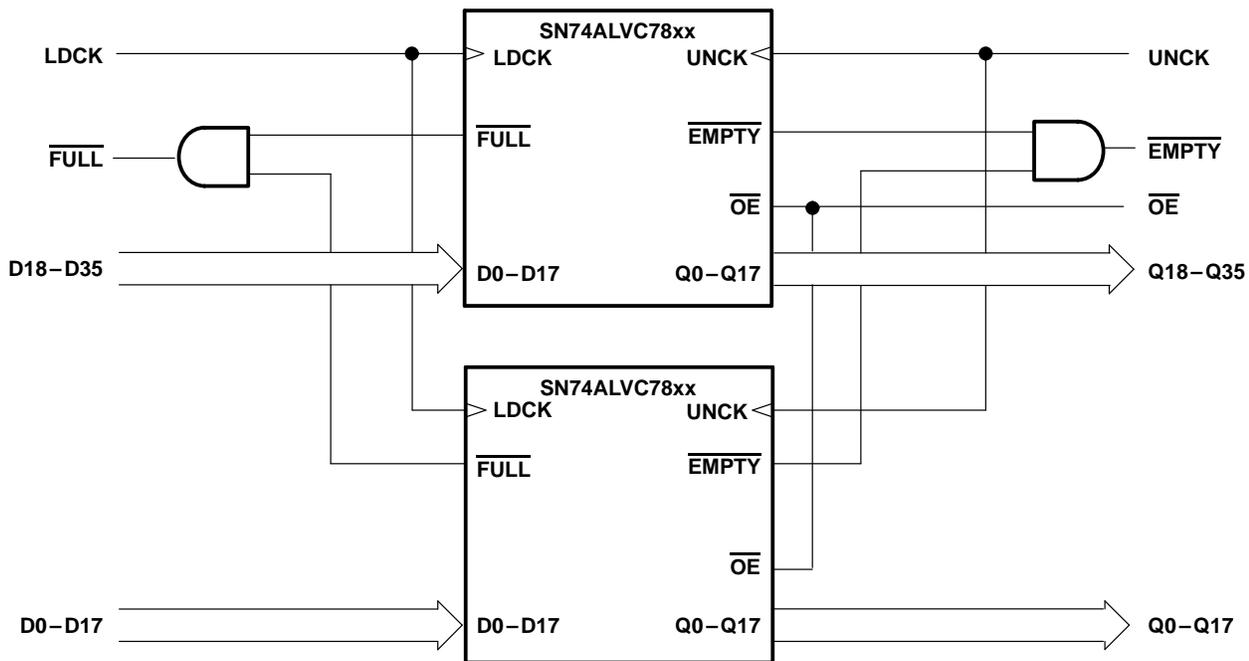


Figure 3. Word-Width Expansion: 512 × 36 Bit, 256 × 36 Bit, and 64 × 36 Bit

TYPICAL CHARACTERISTICS

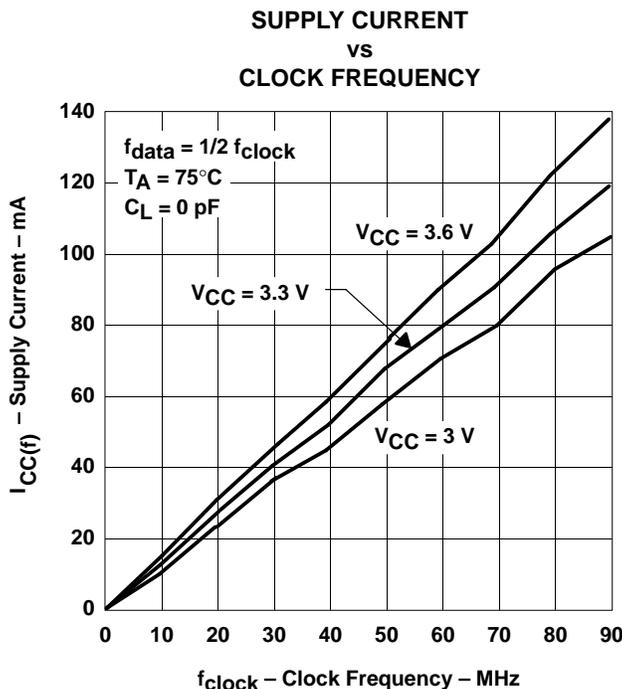


Figure 4

calculating power dissipation

With $I_{CC}(f)$ taken from Figure 4, the dynamic power (P_d) based on all data outputs changing states on each read can be calculated by:

$$P_d = V_{CC} \times [I_{CC}(f) + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate total power (P_T) can be calculated if quiescent power (P_q) is also taken into consideration. Quiescent power (P_q) can be calculated by:

$$P_q = V_{CC} \times [I_{CC}(l) + (N \times \Delta I_{CC} \times dc)]$$

Total power is:

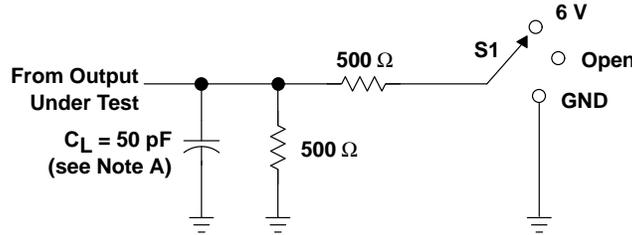
$$P_T = P_d + P_q$$

The above equations provide worst-case power calculations.

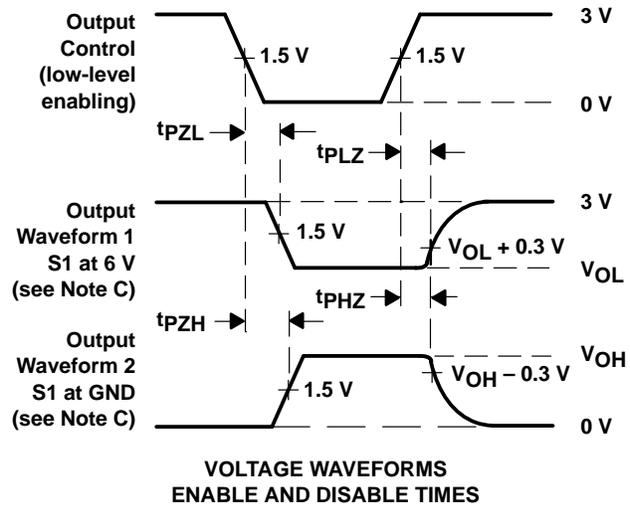
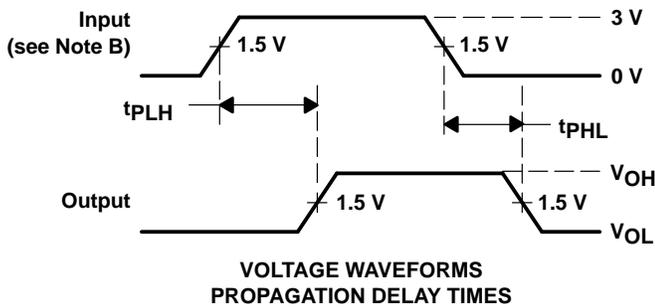
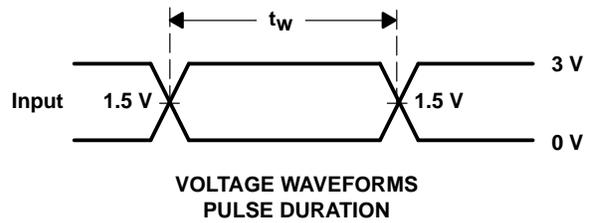
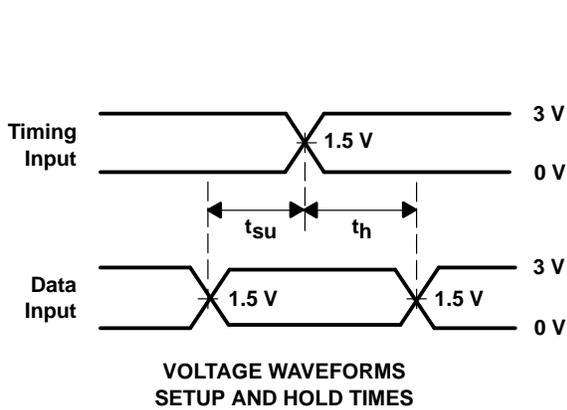
Where:

- N = number of inputs driven by TTL levels
- ΔI_{CC} = increase in power supply current for each input at a TTL high level
- dc = duty cycle of inputs at a TTL high level of 3.4 V
- C_L = output capacitance load
- f_o = switching frequency of an output
- $I_{CC}(l)$ = idle current, supply current when FIFO is idle $\approx pF \times f_{clock} = 0.2 \times f_{clock}$
(current is due to free-running clocks)
- pF = power factor
- $I_{CC}(f)$ = active current, supply current when FIFO is transferring data

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3-STATE OUTPUTS (ANY Q)

PARAMETER		R1, R2	C_L^\dagger	S1
t_{en}	t_{PZH}	500 Ω	50 pF	GND
	t_{PZL}			6 V
t_{dis}	t_{PHZ}	500 Ω	50 pF	GND
	t_{PLZ}			6 V
t_{pd}	t_{PLH}/t_{PHL}	500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 5. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)

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