- **Operates at 3-V to 3.6-V $V_{CC}$**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **Fast Access Times of 13 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **Pin Compatible With SN74ACT7803, SN74ACT7805, and SN74ACT7813**
- **Available in Shrink Small-Outline 300-mil (DL) Package Using 25-mil Center-to-Center Lead Spacing**

**DL PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| $\overline{\text{RESET}}$ | 1 | 56 | $\overline{\text{OE1}}$ |
| D17 | 2 | 55 | Q17 |
| D16 | 3 | 54 | Q16 |
| D15 | 4 | 53 | Q15 |
| D14 | 5 | 52 | GND |
| D13 | 6 | 51 | Q14 |
| D12 | 7 | 50 | $V_{CC}$ |
| D11 | 8 | 49 | Q13 |
| D10 | 9 | 48 | Q12 |
| $V_{CC}$ | 10 | 47 | Q11 |
| D9 | 11 | 46 | Q10 |
| D8 | 12 | 45 | Q9 |
| GND | 13 | 44 | GND |
| D7 | 14 | 43 | Q8 |
| D6 | 15 | 42 | Q7 |
| D5 | 16 | 41 | Q6 |
| D4 | 17 | 40 | Q5 |
| D3 | 18 | 39 | $V_{CC}$ |
| D2 | 19 | 38 | Q4 |
| D1 | 20 | 37 | Q3 |
| D0 | 21 | 36 | Q2 |
| HF | 22 | 35 | GND |
| $\overline{\text{PEN}}$ | 23 | 34 | Q1 |
| AF/AE | 24 | 33 | Q0 |
| WRTCLK | 25 | 32 | RDCLK |
| $\overline{\text{WRTEN2}}$ | 26 | 31 | $\overline{\text{RDEN}}$ |
| WRTEN1 | 27 | 30 | $\overline{\text{OE2}}$ |
| IR | 28 | 29 | OR |

## description

The SN74ALVC7803, SN74ALVC7805, and SN74ALVC7813 are FIFOs suited for buffering asynchronous data paths at 50-MHz clock rates and 13-ns access times. These devices are designed for 3-V to 3.6-V $V_{CC}$ operation. The 56-pin shrink small-outline (DL) package offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic.

The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ALVC7803, SN74ALVC7805, and SN74ALVC7813 are characterized for operation from 0°C to 70°C.

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**TEXAS INSTRUMENTS**

## logic symbol†
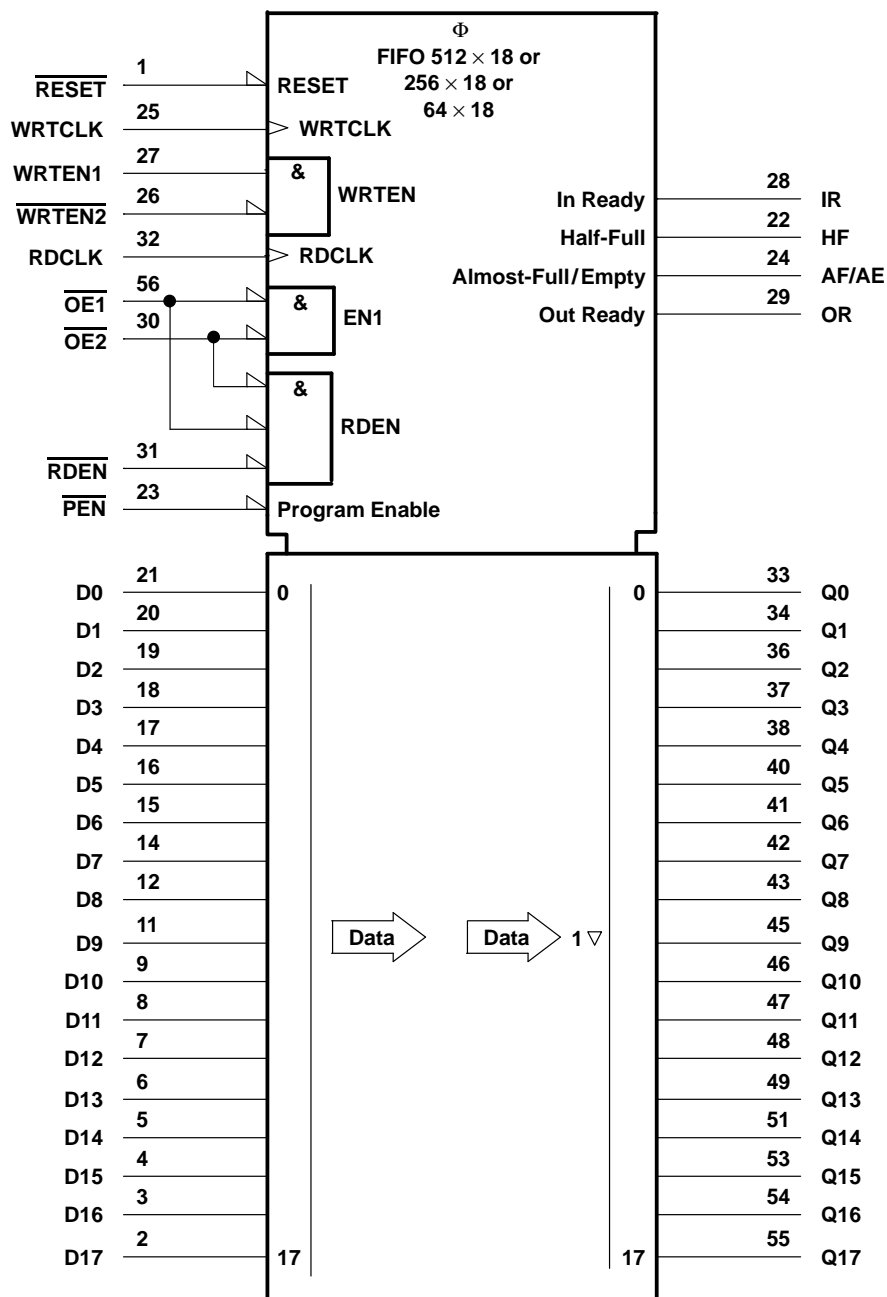


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

![Texas Instruments logo] **TEXAS INSTRUMENTS**

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**functional block diagram**
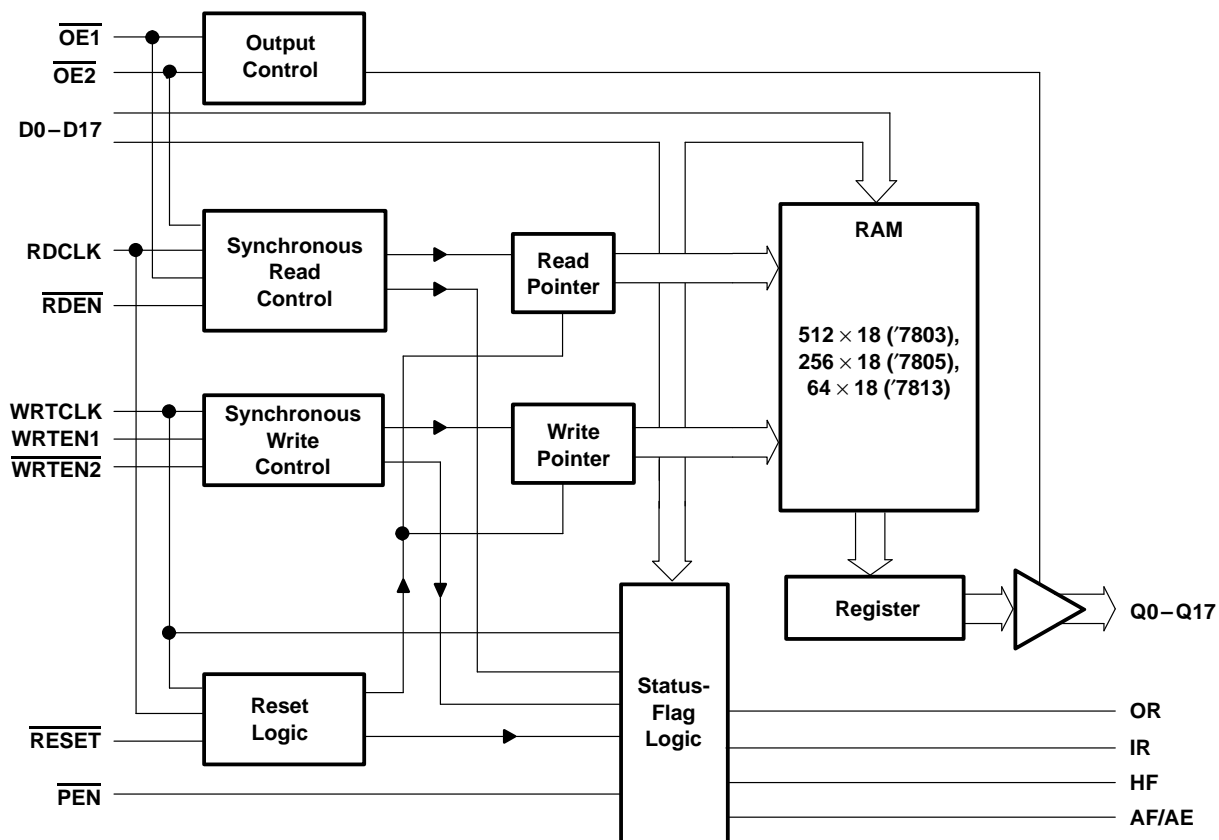
## Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AF/AE | 24 | O | Almost-full/almost-empty flag. Depth-offset values can be programmed for this flag, or the default value of 64 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (512 minus Y) or more words. AF/AE is high after reset. |
| D0–D17 | 2–9, 11–12, 14–21 | I | 18-bit data input port |
| HF | 22 | O | Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset. |
| IR | 28 | O | Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset. |
| $\overline{OE1}$, $\overline{OE2}$ | 56, 30 | I | Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled and the data outputs are in the high-impedance state. |
| OR | 29 | O | Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory. |
| $\overline{PEN}$ | 23 | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high. |
| Q0–Q17 | 33–34, 36–38, 40–43, 45–49, 51, 53–55 | O | 18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17. |
| RDCLK | 32 | I | Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK. |
| $\overline{RDEN}$ | 31 | I | Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK. |
| $\overline{RESET}$ | 1 | I | Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high. |
| WRTCLK | 25 | I | Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK. |
| WRTEN1, $\overline{WRTEN2}$ | 27, 26 | I | Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK. |

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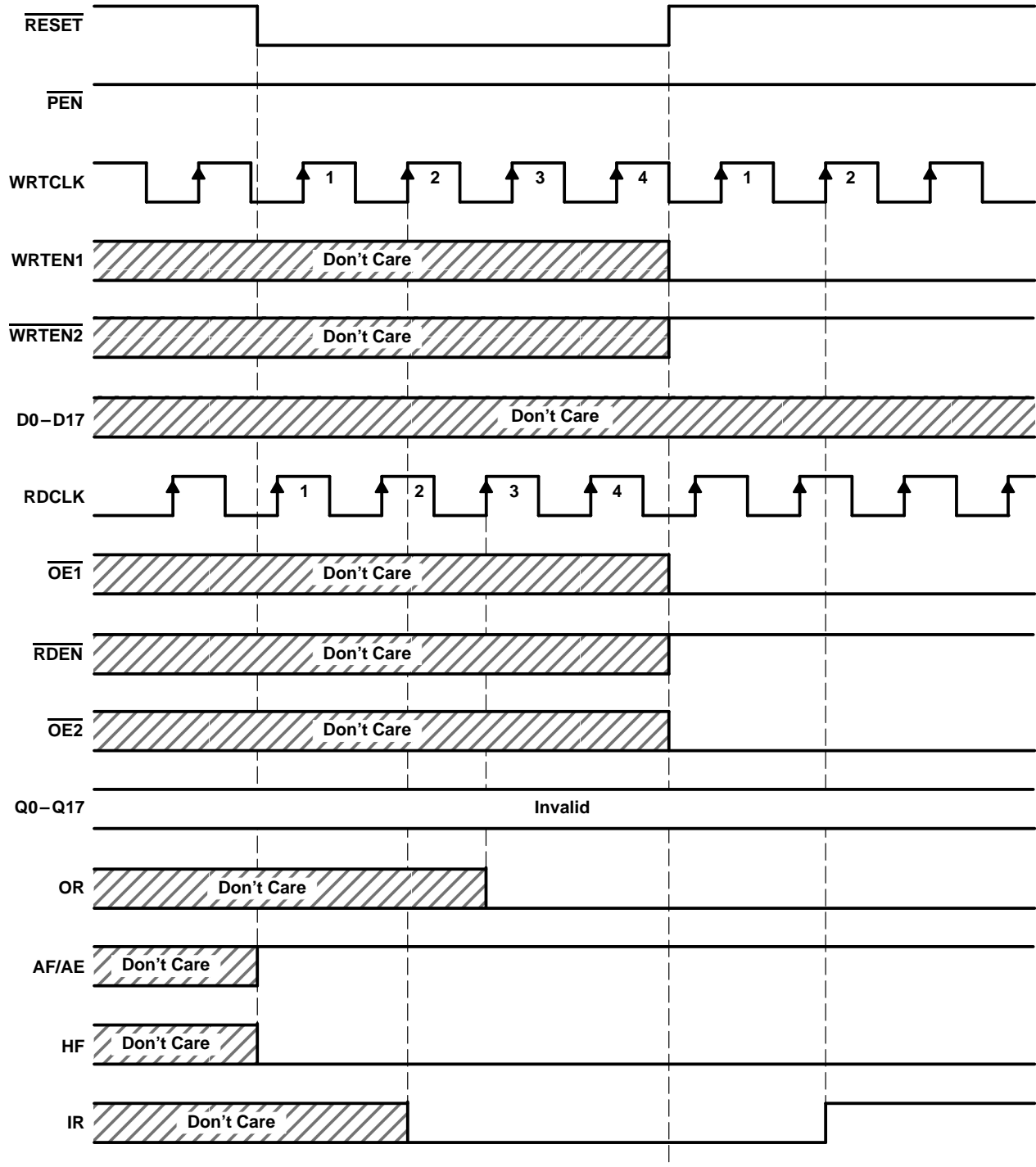
Define the AF/AE Flag Using the Default Value of X = Y = 64

**Figure 1. Reset Cycle**
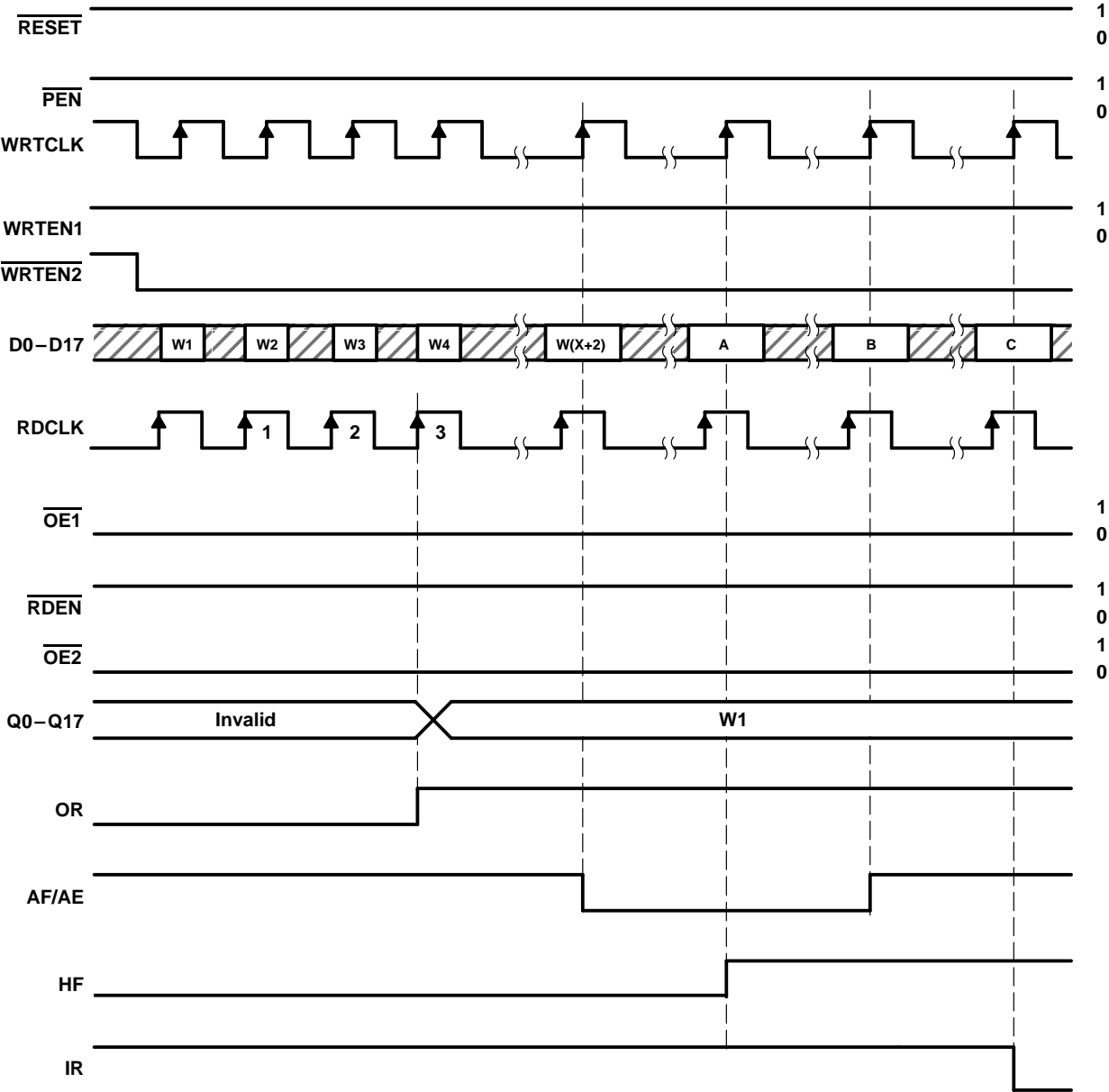
**DATA WORD NUMBER FOR FLAG TRANSITIONS**

| DEVICE | TRANSITION WORD | | |
|---|---|---|---|
| | **A** | **B** | **C** |
| SN74ALVC7803 | W257 | W(513−Y) | W513 |
| SN74ALVC7805 | W129 | W(257−Y) | W257 |
| SN74ALVC7813 | W33 | W(65−Y) | W65 |

**Figure 2. FIFO Write**
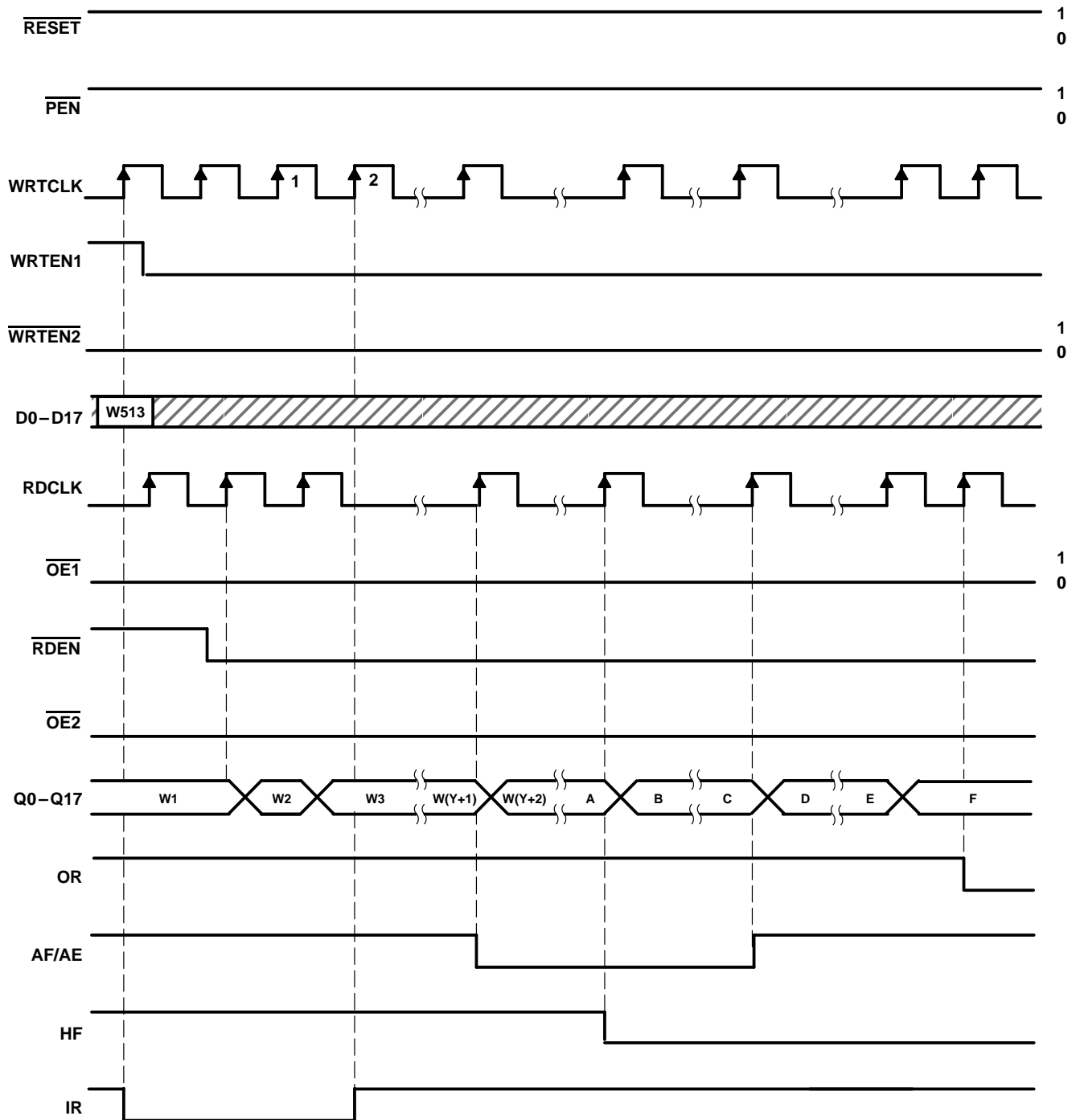
**DATA WORD NUMBERS FOR FLAG TRANSITIONS**

| DEVICE | TRANSITION WORD | | | | | |
|---|---|---|---|---|---|---|
| | **A** | **B** | **C** | **D** | **E** | **F** |
| SN74ALVC7803 | W257 | W258 | W(512−X) | W(513−X) | W512 | W513 |
| SN74ALVC7805 | W129 | W130 | W(256−X) | W(257−X) | W256 | W257 |
| SN74ALVC7813 | W33 | W34 | W(64−X) | W(65−X) | 64 | 65 |

**Figure 3. FIFO Read**

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## offset values for AF/AE

The almost-full/almost-empty (AF/AE) flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 64 are used. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words.

Program enable ($\overline{\text{PEN}}$) should be held high throughout the reset cycle. $\overline{\text{PEN}}$ can be brought low only when IR is high. On the following low-to-high transition of WRTCLK, the binary value on D0–D7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D7 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{\text{WRTEN2}}$). A maximum value of 255 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 64, $\overline{\text{PEN}}$ must be held high.
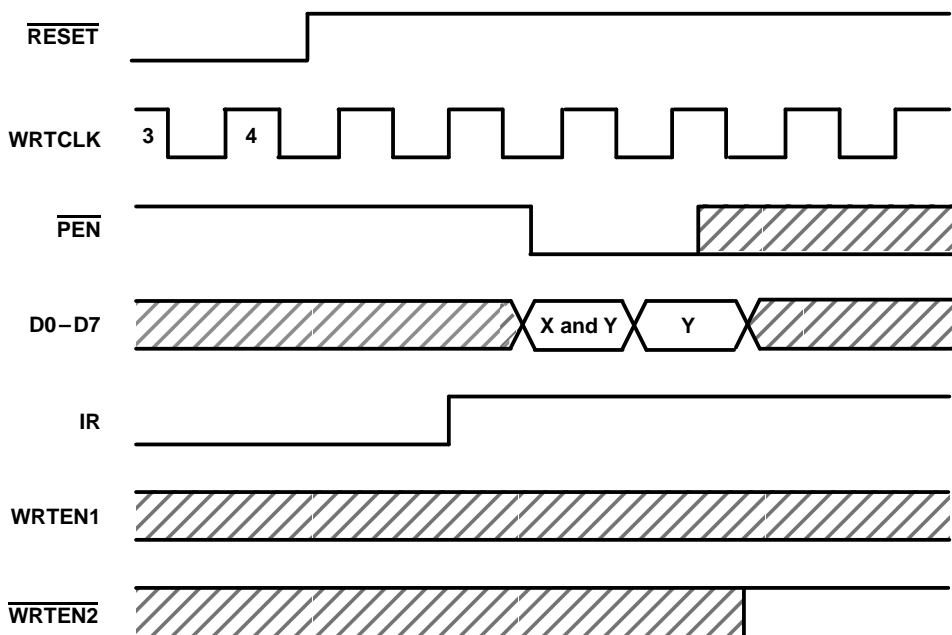


**Figure 4. Programming X and Y Separately**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ......................................................... −0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) ................................................. −0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2) ................................... −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) ................................................. −50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) ................................ ±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) ................................... ±50 mA
Continuous current through $V_{CC}$ or GND ............................................. ±100 mA
Voltage applied to a disabled 3-state output ........................................... 3.6 V
Operating free-air temperature range, $T_A$ ........................................... 0°C to 70°C
Storage temperature range, $T_{stg}$ .................................................. −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.

TEXAS
INSTRUMENTS

## recommended operating conditions

| | | | SN74ALVC7803-20 SN74ALVC7805-20 SN74ALVC7813-20 $V_{CC}$ = 3.3 V ± 0.3 V | | SN74ALVC7803-25 SN74ALVC7805-25 SN74ALVC7813-25 $V_{CC}$ = 3.3 V ± 0.3 V | | SN74ALVC7803-40 SN74ALVC7805-40 SN74ALVC7813-40 $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | V |
| $V_{II}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current, Q outputs, Flags | $V_{CC}$ = 3 V | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current, Q outputs, Flags | $V_{CC}$ = 3 V | | 16 | | 16 | | 16 | mA |
| $f_{clock}$ | Clock frequency | | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | D0–D17 high or low | 9 | | 10 | | 14 | | ns |
| | | WRTCLK high or low | 7 | | 8 | | 12 | | |
| | | RDCLK high or low | 7 | | 8 | | 12 | | |
| | | $\overline{PEN}$ low | 9 | | 9 | | 12 | | |
| | | WRTEN1 high, $\overline{WRTEN2}$ low | 8 | | 8 | | 12 | | |
| | | $\overline{OE1}$, $\overline{OE2}$ low | 9 | | 9 | | 12 | | |
| | | $\overline{RDEN}$ low | 8 | | 8 | | 12 | | |
| $t_{su}$ | Setup time | D0–D17 before WRTCLK↑ | 5 | | 5 | | 5 | | ns |
| | | WRTEN1, $\overline{WRTEN2}$ before WRTCLK↑ | 5 | | 5 | | 5 | | |
| | | $\overline{OE1}$, $\overline{OE2}$ before RDCLK↑ | 5 | | 6 | | 6 | | |
| | | $\overline{RDEN}$ before RDCLK↑ | 5 | | 5 | | 7 | | |
| | | Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑† | 6 | | 6 | | 6 | | |
| | | $\overline{PEN}$ before WRTCLK↑ | 6 | | 6 | | 6 | | |
| $t_h$ | Hold time | D0–D17 after WRTCLK↑ | 0 | | 0 | | 0 | | ns |
| | | WRTEN1, $\overline{WRTEN2}$ after WRTCLK↑ | 0 | | 0 | | 0 | | |
| | | $\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑ | 0 | | 0 | | 0 | | |
| | | Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑† | 2 | | 2 | | 2 | | |
| | | $\overline{PEN}$ low after WRTCLK↑ | 2 | | 2 | | 2 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | °C |

† To permit the clock pulse to be utilized for reset purposes

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3 V, | $I_{IK}$ = − 18 mA | | | −1.2 | V |
| $V_{OH}$ | Flags, Q outputs | $V_{CC}$ = MIN to MAX, | $I_{OH}$ = −100 µA | $V_{CC}$ − 0.2 | | | V |
| | | $V_{CC}$ = 3 V, | $I_{OH}$ = −8 mA | 2.4 | | | |
| $V_{OL}$ | Flags, Q outputs | $V_{CC}$ = MIN to MAX, | $I_{OL}$ = 100 µA | | | 0.2 | V |
| | Flags | $V_{CC}$ = 3 V, | $I_{OL}$ = 8 mA | | | 0.4 | |
| | Q outputs | $V_{CC}$ = 3 V, | $I_{OL}$ = 16 mA | | | 0.55 | |
| $I_I$ | | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±5 | µA |
| $I_{OZ}$ | | $V_{CC}$ = 3.6 V, | $V_O$ = $V_{CC}$ or GND | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or 0 | | | | 40 | µA |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 3.6 V, One input at $V_{CC}$ − 0.6 V | Other inputs at $V_{CC}$ or GND, | | | 500 | µA |
| $C_i$ | | $V_{CC}$ = 3.3 V, | $V_I$ = $V_{CC}$ or GND | | 2.5 | | pF |
| $C_o$ | | $V_{CC}$ = 3.3 V, | $V_O$ = $V_{CC}$ or GND | | 5.5 | | pF |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 7)

| PARAMETER | FROM (OUTPUT) | TO (INPUT) | SN74ALVC7803-20 SN74ALVC7805-20 SN74ALVC7813-20 $V_{CC}$ = 3.3 V ± 0.3 V | | SN74ALVC7803-25 SN74ALVC7805-25 SN74ALVC7813-25 $V_{CC}$ = 3.3 V ± 0.3 V | | SN74ALVC7803-40 SN74ALVC7805-40 SN74ALVC7813-40 $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | WRTCLK or RDCLK | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | RDCLK↑ | Any Q | 4 | 13 | 4 | 15 | 4 | 20 | ns |
| $t_{pd}$ | WRTCLK↑ | IR | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | RDCLK↑ | OR | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | WRTCLK↑ | AF/AE | 7 | 19 | 7 | 21 | 7 | 23 | ns |
| $t_{pd}$ | RDCLK↑ | AF/AE | 7 | 19 | 7 | 21 | 7 | 23 | ns |
| $t_{PLH}$ | WRTCLK↑ | HF | 7 | 17 | 7 | 19 | 7 | 21 | ns |
| $t_{PHL}$ | RDCLK↑ | | 7 | 18 | 7 | 20 | 7 | 22 | |
| $t_{PLH}$ | $\overline{RESET}$ low | AF/AE | 2 | 11 | 2 | 13 | 2 | 15 | ns |
| $t_{PHL}$ | | HF | 2 | 12 | 2 | 14 | 2 | 16 | |
| $t_{en}$ | $\overline{OE1}$, $\overline{OE2}$ | Any Q | 2 | 11 | 2 | 11 | 2 | 14 | ns |
| $t_{dis}$ | | | 2 | 11 | 2 | 14 | 2 | 14 | |

## operating characteristics, $V_{CC}$ = 3.3 V, $T_A$ = 25°C

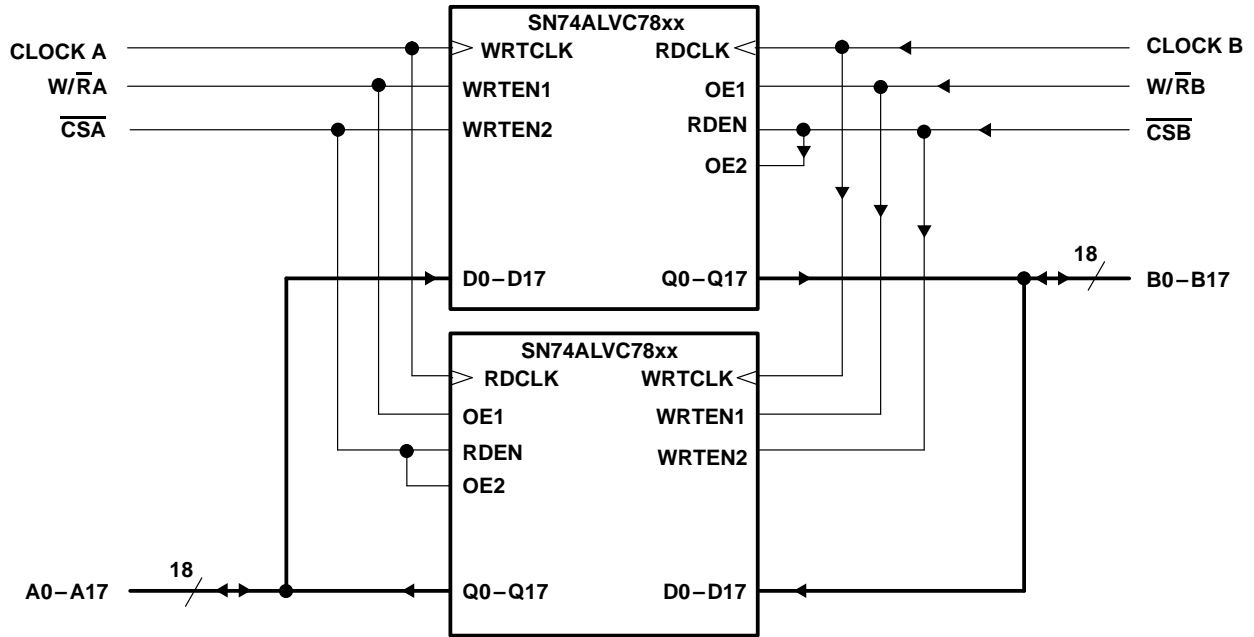| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 5 MHz | 53 | pF |

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## APPLICATION INFORMATION



**Figure 5. Bidirectional Configuration**
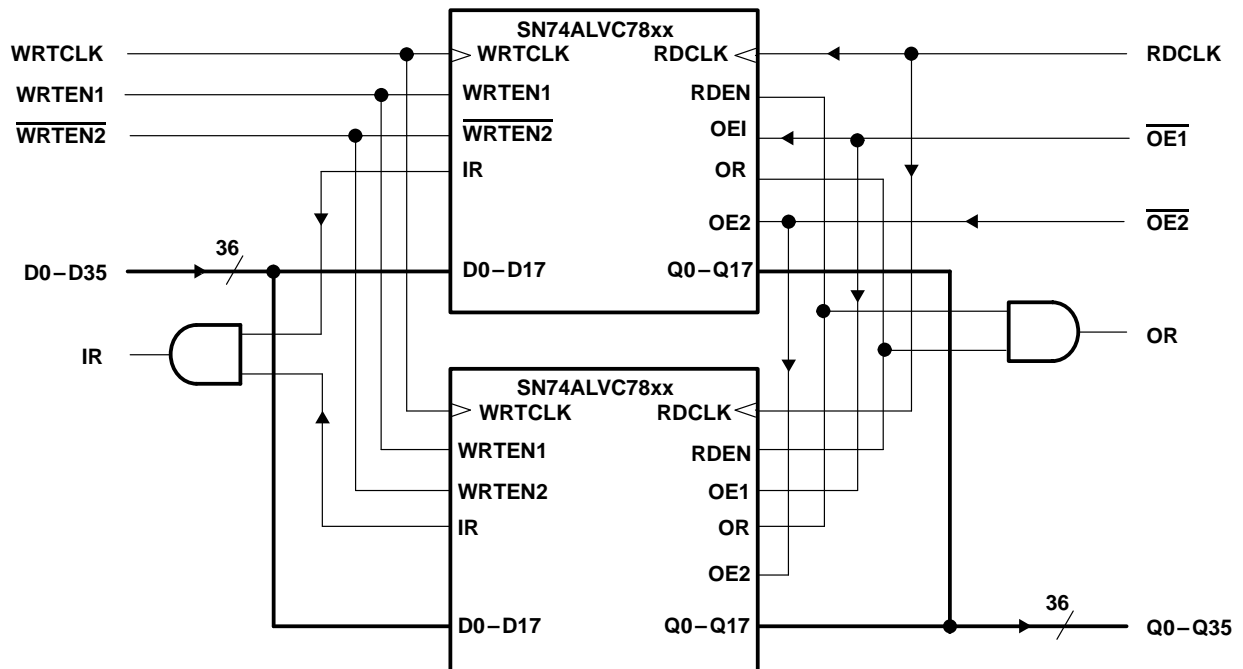


**Figure 6. Word-Width Expansion: 512 × 36 Bit , 256 × 36 Bit, and 64 × 36 Bit**

## TYPICAL CHARACTERISTICS
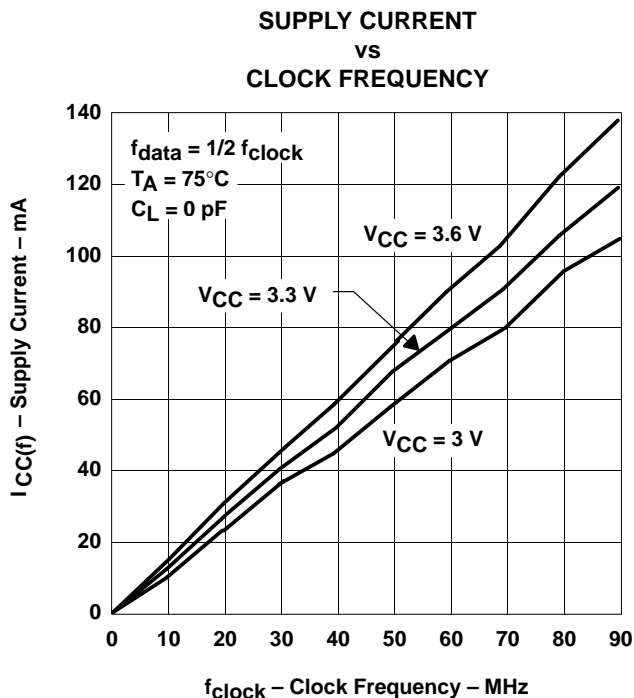
**SUPPLY CURRENT**
**vs**
**CLOCK FREQUENCY**



**Figure 7**

## calculating power dissipation

With $I_{CC(f)}$ taken from Figure 7, the dynamic power ($P_d$), based on all data outputs changing states on each read, can be calculated by:

$$P_d = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate total power ($P_T$) can be calculated if quiescent power (Pq) is also taken into consideration. Quiescent power ($P_q$) can be calculated by:

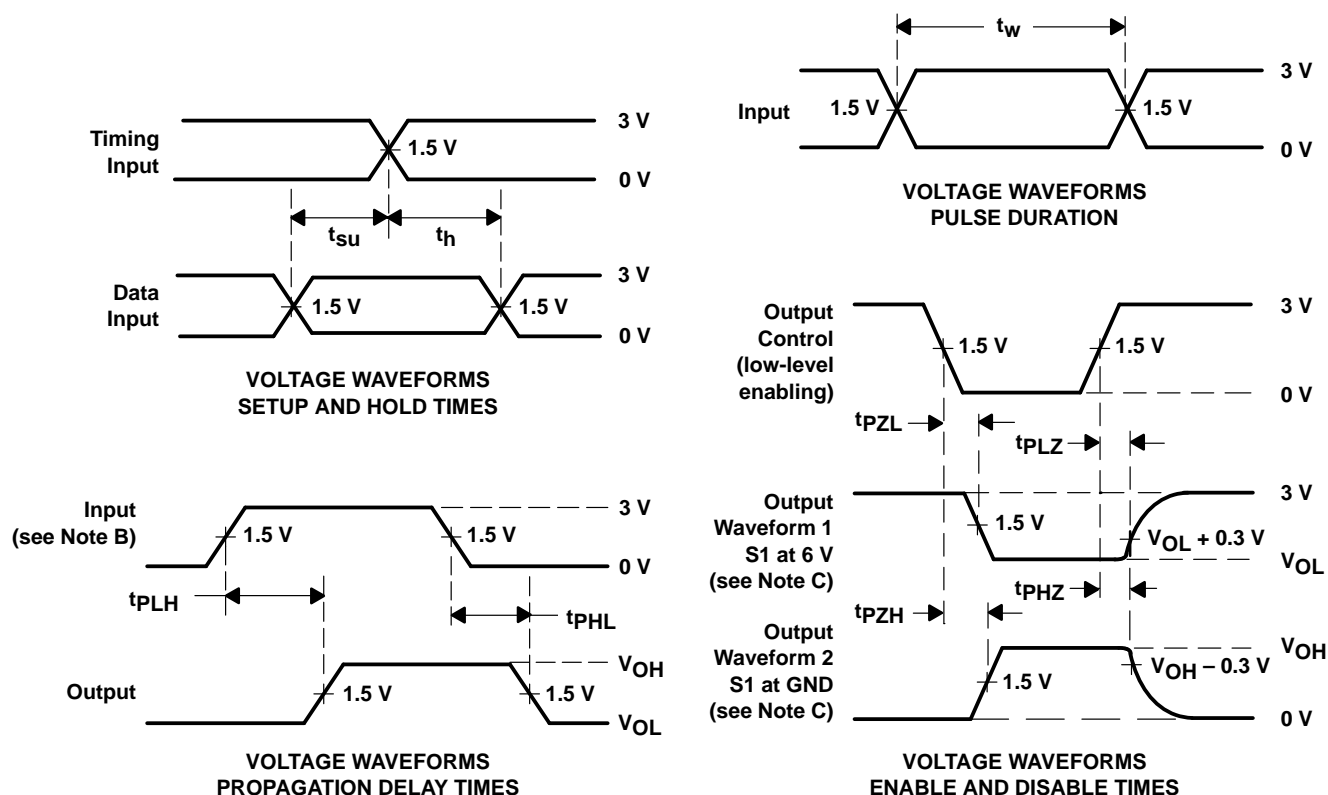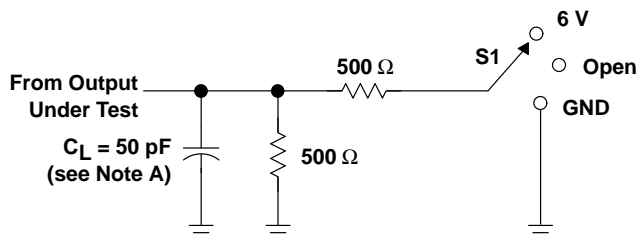$$P_q = V_{CC} \times [I_{CC(I)} + (N \times \Delta I_{CC} \times dc)]$$

Total power would be:

$$P_T = P_d + P_q$$

The above equations provide worst-case power calculations.

Where:

$N$ = number of inputs driven by TTL levels
$\Delta I_{CC}$ = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_L$ = output capacitance load
$f_o$ = switching frequency of an output
$I_{CC(I)}$ = idle current, supply current when FIFO is idle $\approx$ pF $\times f_{clock} = 0.2 \times f_{clock}$
  (current is due to free-running clocks)
pF = power factor (the slope of idle current versus clock frequency)
$I_{CC(f)}$ = active current, supply current when FIFO is transferring data

## PARAMETER MEASUREMENT INFORMATION



**LOAD CIRCUIT FOR OUTPUTS**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

NOTES: A. $C_L$ includes probe and jig capacitance.
      B. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O$ = 50 $\Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
      C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
        Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

**3-STATE OUTPUTS (ANY Q)**

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 $\Omega$ | 50 pF | GND |
| | $t_{PZL}$ | | | 6 V |
| $t_{dis}$ | $t_{PHZ}$ | 500 $\Omega$ | 50 pF | GND |
| | $t_{PLZ}$ | | | 6 V |
| $t_{pd}$ | $t_{PLH}/t_{PHL}$ | 500 $\Omega$ | 50 pF | Open |

† Includes probe and test-fixture capacitance

**Figure 8. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)**

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