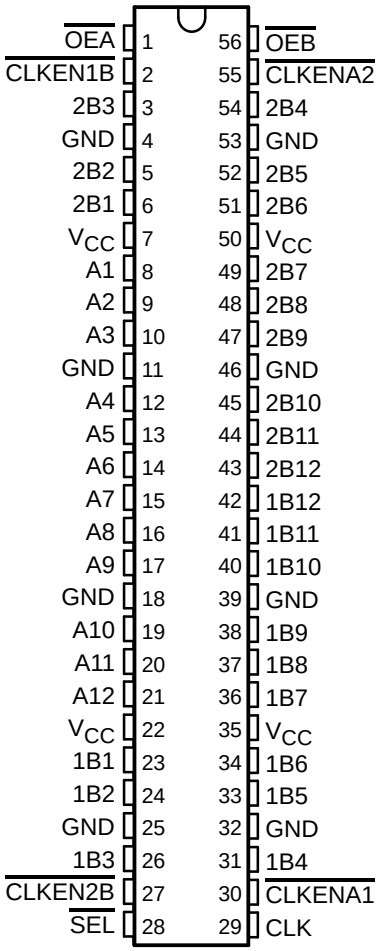
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16270 is a 12-bit to 24-bit registered bus exchanger, which is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3 V) V_{CC} operation.

The device provides for synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate $\overline{\text{CLKEN}}$ inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A to 1B path, with a single storage register in the A to 2B path. Proper control of the $\overline{\text{CLKENA}}$ inputs allow two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$). These control pins are registered so that bus direction changes are synchronous with the clock.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16270 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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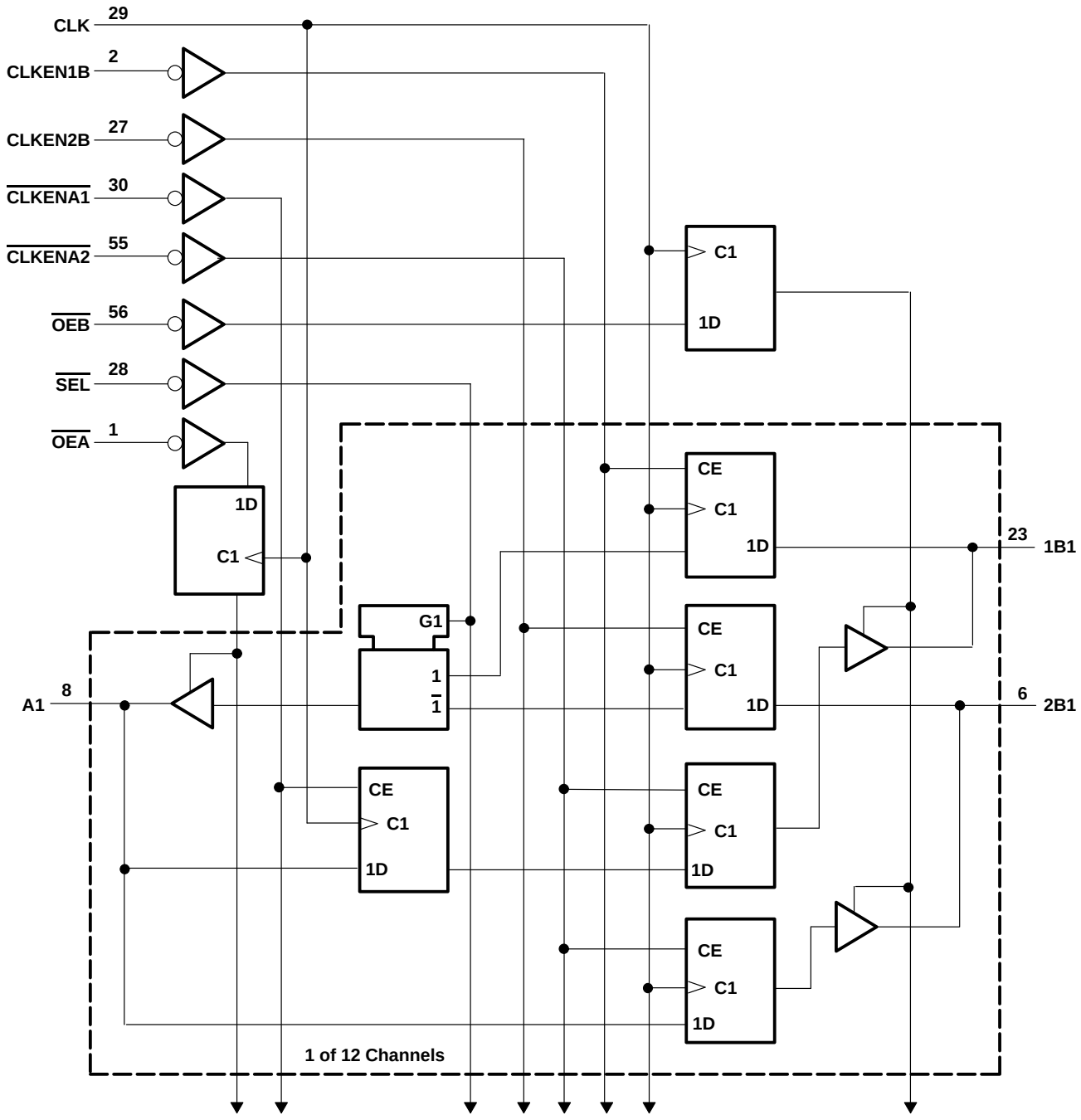
PRODUCT PREVIEW

logic diagram (positive logic)



Function Tables

OUTPUT-ENABLE TABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L[1]	X
L	X	↑	H	H[1]	X
X	L	↑	L	X	L
X	L	↑	H	X	H

[1] Two CLK edges are needed to propagate data.

B-TO-A STORAGE TABLE ($\overline{OEA}$ = L)

INPUTS						OUTPUT
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	A
H	X	X	H	X	X	A_0†
X	H	X	L	X	X	A_0†
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I	Inputs	$V_I = V_{CC}$ or GND	3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		–75		
I_{OZ}		$V_O = V_{CC}$ or GND	3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μA
C_i		$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}		$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

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