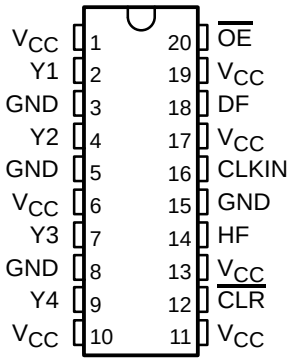
- **Replaces SN74ABT338**
- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **TTL-Compatible Inputs and TTL Outputs**
- **Distributes One Clock Input to Six Outputs**
  - **Four Same-Frequency Outputs**
  - **One Half-Frequency Outputs**
  - **One Double-Frequency Output**
- **Output Duty Cycle Correction to 50%**
- **No External RC Network Required**
- **Edge-Triggered Clear for Half-Frequency Output**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **Packaged in Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)



description

The CDC338 is a high-performance, low-skew, low-jitter clock driver. It uses phase-lock loops (PLLs) to precisely align, in both frequency and phase, the clock output signals to the clock (CLKIN) input signal. It is specifically designed for use with popular microprocessors operating at speeds from 15 MHz to 35 MHz or up to 70 MHz using the double-frequency (DF) output.

The four Y outputs switch in phase and at the same frequency as CLKIN. The half-frequency (HF) output operates at one-half the CLKIN frequency, and DF operates at twice the CLKIN frequency. All output signal duty cycles are adjusted to 50% independent of the duty cycle at CLKIN.

Output-enable ($\overline{OE}$) and clear ($\overline{CLR}$) inputs are also provided for output control and synchronization. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. The $\overline{CLR}$ input is negative-edge-triggered and is provided to allow phase synchronization of the HF outputs on multiple CDC338 devices.

Unlike many products containing PLLs, the CDC338 does not require external RC networks. The loop filter for each PLL is included on chip, minimizing component count, board space, and cost. Additionally, each output has its own PLL, which allows mismatches between loads from one output to another.

Because it is based on PLL circuitry, the CDC338 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN as well as following any changes to the PLL reference or feedback signals. Such changes occur upon phase reset of the HF output and upon enable of all outputs. Therefore, stabilization is also required following high-to-low transitions on either $\overline{CLR}$ or $\overline{OE}$.

The CDC338 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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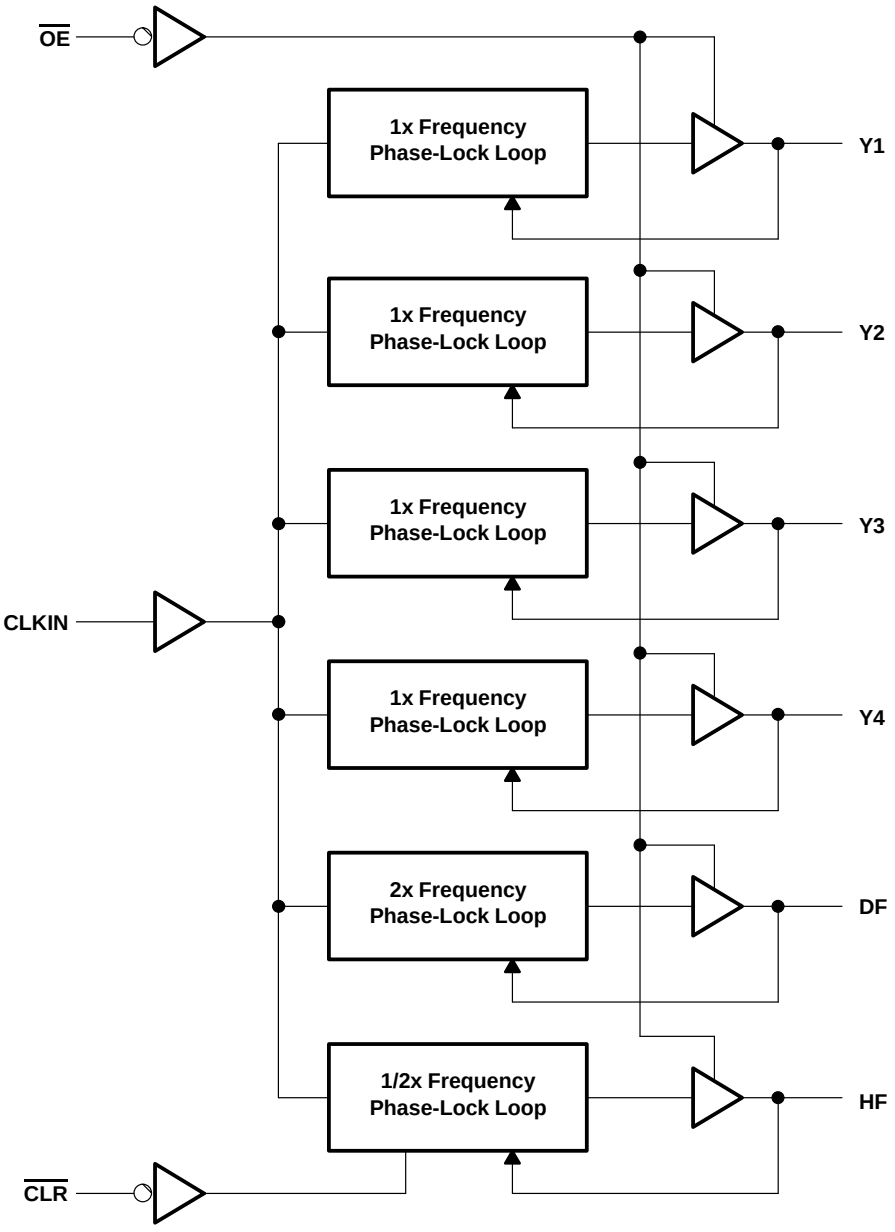
PRODUCT PREVIEW

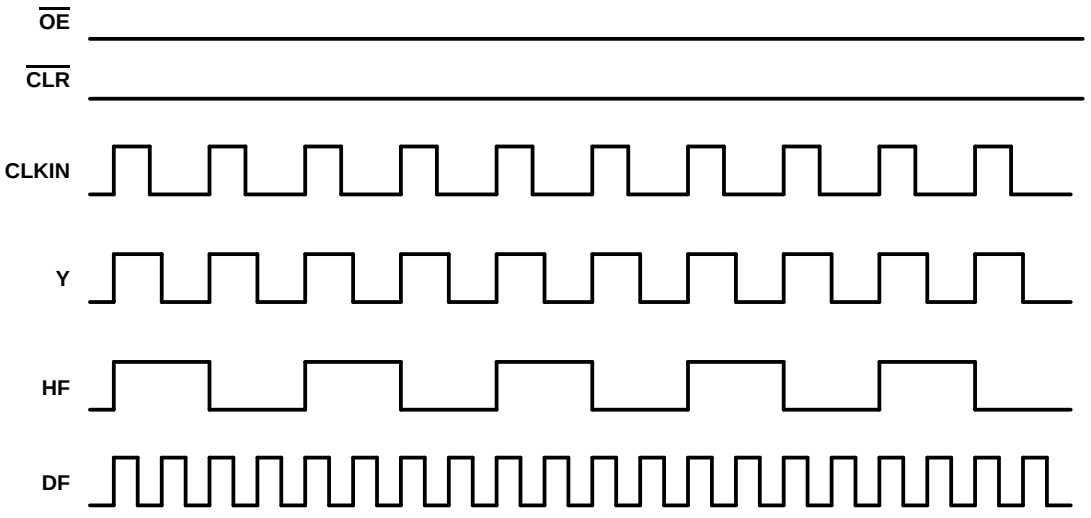
functional block diagram



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
CLKIN	16	I	This input pin provides the clock signal to be distributed by the CDC338 clock driver circuit. This clock signal is used to provide the reference signals to the integrated phase-lock loops that generate the clock-output signals. This signal must have a fixed frequency and fixed phase in order for these phase-lock loops to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the phase-lock loops to phase lock their feedback signals to their reference signals.
$\overline{\text{CLR}}$	12	I	This input pin is used to reset the HF output signal to a known phase. It is useful to ensure that HF output signals of multiple CDC338 circuits are all in the same phase. The $\overline{\text{CLR}}$ signal is a negative-edge-triggered signal. When a high-to-low edge occurs at $\overline{\text{CLR}}$, the flip-flop that divides the CLKIN signal to provide reference for the HF phase-lock loop is asynchronously cleared to a low level. Following the required stabilization time, HF output signals for all CDC338 units that receive the same CLKIN and $\overline{\text{CLR}}$ signals will have the same phase. In order for the clear function to operate in a deterministic fashion, the circuit must be allowed to stabilize from power up before using this function.
DF	18	O	This output pin is used to transmit a double-frequency clock signal. This signal is phase locked to the CLKIN signal via a phase-lock loop that operates at twice the frequency of the reference CLKIN signal. Due to normal operation of the phase-lock loop, the duty cycle of the DF signal will be nominally 50% independent of the duty cycle of the CLKIN signal.
HF	14	O	This output pin is used to transmit a half-frequency clock signal. This signal is phase locked to the CLKIN signal via a phase-lock loop that operates at half the frequency of the reference CLKIN signal. Due to normal operation of the phase-lock loop, the duty cycle of the HF signal will be nominally 50% independent of the duty cycle of the CLKIN signal. Since the phase of the HF signal cannot be determined at power up, the $\overline{\text{CLR}}$ input has been provided to allow the HF signals of multiple CDC338 circuits to be reset to the same phase.
$\overline{\text{OE}}$	20	I	This input pin is the output enable for all outputs. When $\overline{\text{OE}}$ is low, all outputs are enabled. When $\overline{\text{OE}}$ is high, all outputs are in the high-impedance state. Since the feedback signal for each phase-lock loop is taken directly from the appropriate output pin, placing the outputs in the high-impedance state interrupts the feedback loop. Therefore, when a high-to-low transition occurs at $\overline{\text{OE}}$, enabling the output buffers, a stabilization time is required before the phase-lock loops obtain phase lock.
Y1–Y4	2, 4, 7, 9	O	These output pins are used to transmit same-frequency clock signals. These signals are each phase locked to the CLKIN signal via individual phase-lock loops that operate at the same frequency as the reference CLKIN signal. Due to normal operation of the phase-lock loop, the duty cycle of the Y output signals will be nominally 50% independent of the duty cycle of the CLKIN signal.

timing diagram



NOTE: This diagram is applicable only after any appropriate stabilization time has elapsed.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –1.2 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 96 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–48	mA
I_{OL}	Low-level output current		48	mA
T_A	Operating free-air temperature	–40	85	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 3 mA		2.5			V
	V_{CC} = 4.75 V,	I_{OH} = – 48 mA		2			
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA				0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1	µA
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				50	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.5 V				–50	µA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			75	mA
			Outputs low			100	
			Outputs disabled			70	
C_i	V_I = 2.5 V or 0.5 V						pF
C_o	V_O = VCC or GND						pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		15	35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	5		ns
	Input clock duty cycle		40%	60%	
$t_{stabilize}$†	Stabilization time	After $\overline{CLR}\downarrow$	50		µs
		After $\overline{OE}\downarrow$	50		
		After power up	50		

NOTE 3: Preliminary specifications based on SPICE analysis.

† Time required for the integrated phase-lock loop circuits to obtain phase-lock of their feedback signals to their reference signals. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

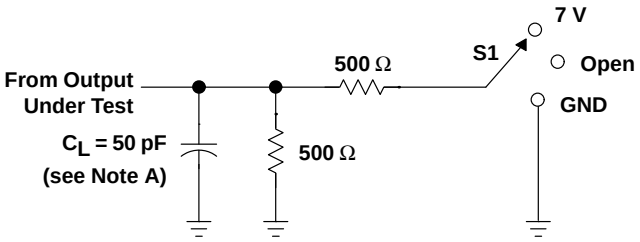
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			35		MHz
t_{PLH}	CLKIN↑	DF, HF, or Y		±1	ns
t_{PHL}		HF		±1	
$t_{sk(o)}$	CLKIN	DF, HF, or Y		0.5	ns
DC		DF, HF, or Y	45%	55%	
t_r					ns
t_f					ns

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

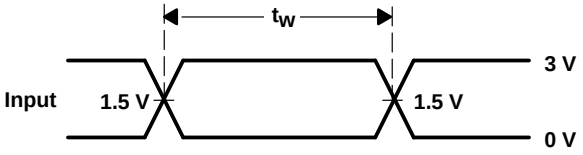
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

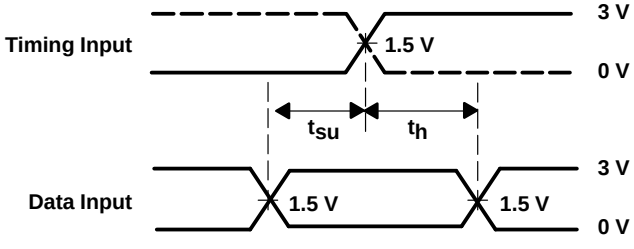


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

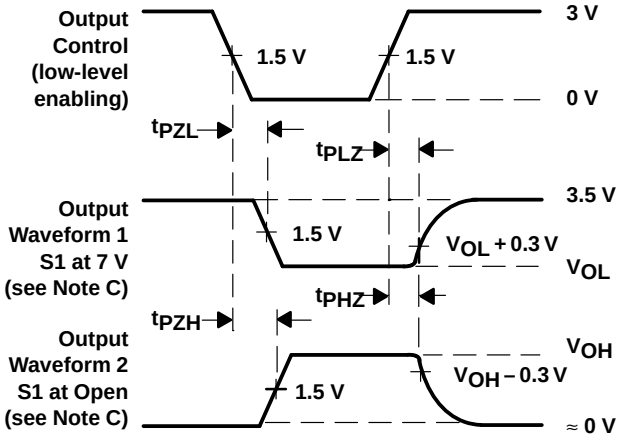
LOAD CIRCUIT FOR OUTPUTS



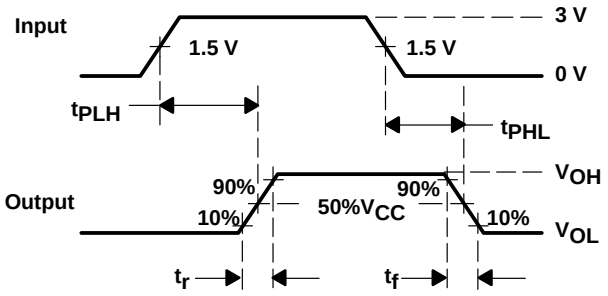
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



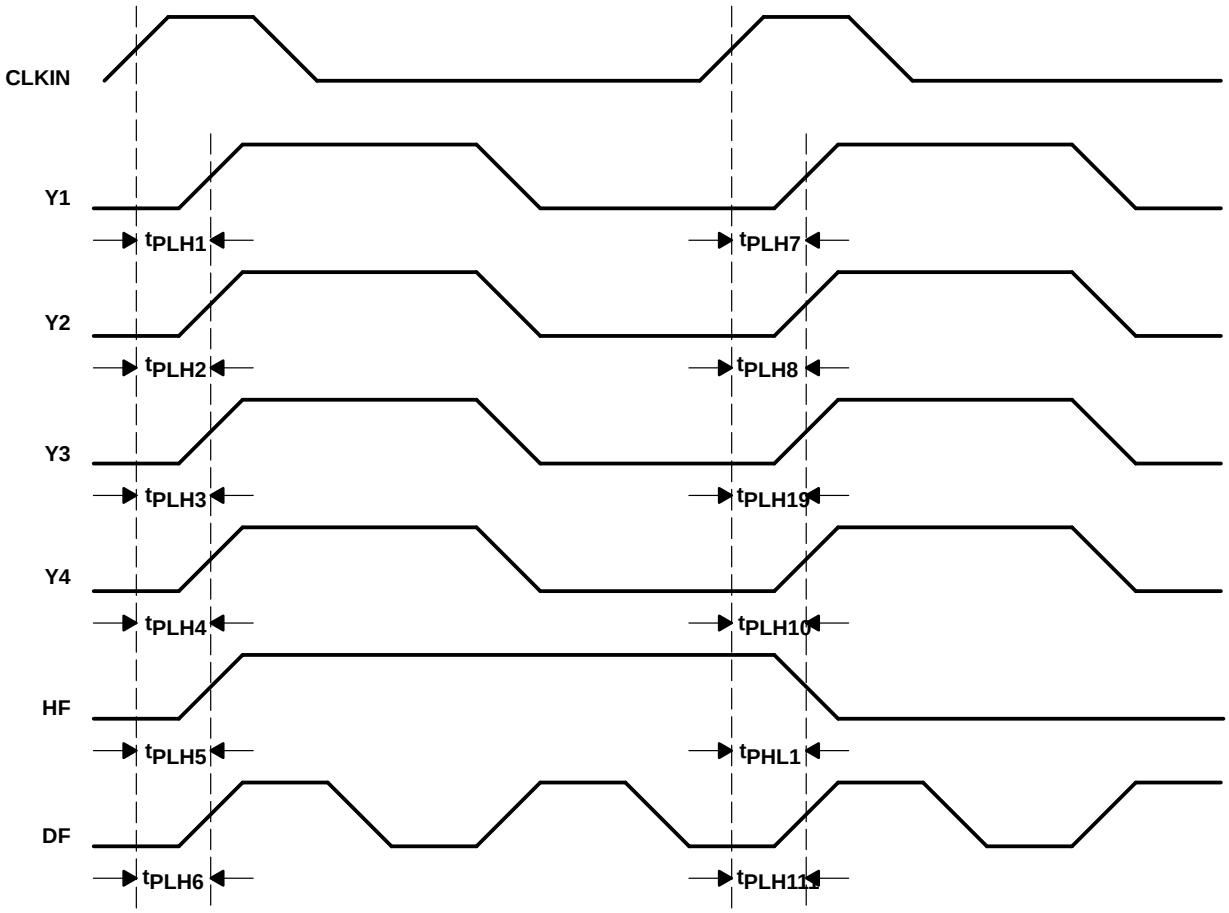
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



Output skew, $t_{sk(o)}$, is calculated as the greater of:
a) the difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . 6), and
b) the difference between the fastest and slowest of t_{PLHn} (n = 7, 8, 9, 10, 11) and t_{PHL1}.

Figure 2. Skew Waveforms and Calculations

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