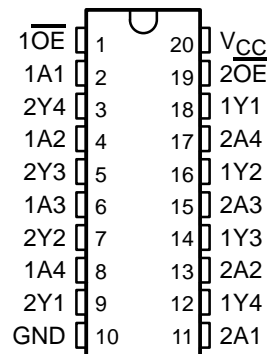


SN74LVC244A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS414F – NOVEMBER 1992 – REVISED JULY 1997

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Shrink Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC244A is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC244A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |



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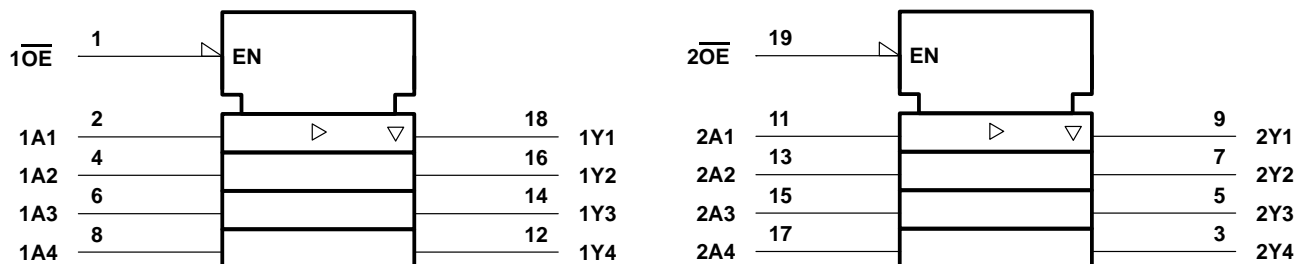
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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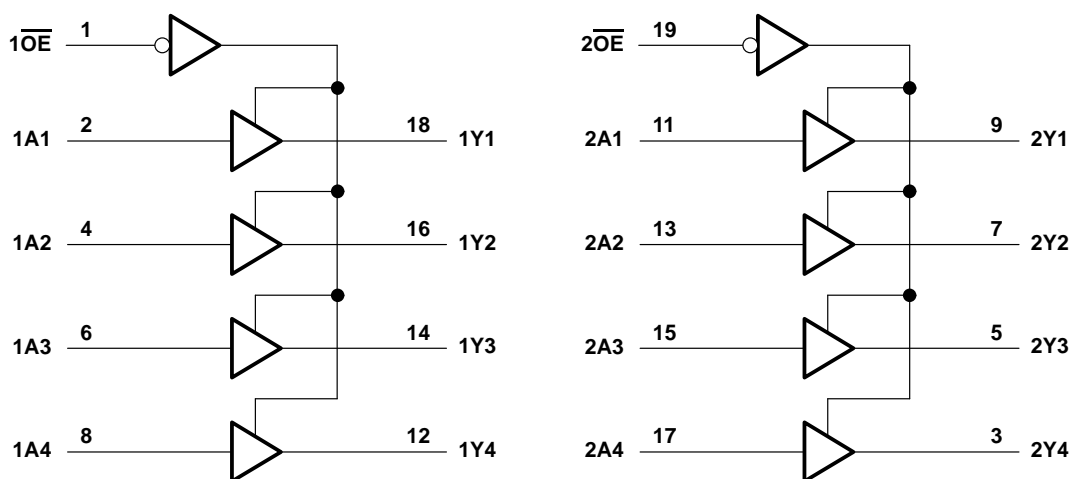
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 6.5 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 6.5 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 6.5 V |
| Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) (see Note 2) | ±50 mA |
| Continuous current through V_{CC} or GND | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): | |
| DB package | 115°C/W |
| DW package | 97°C/W |
| PW package | 128°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC244A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCAS414F – NOVEMBER 1992 – REVISED JULY 1997

recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|----------|--------------------------------|---|-----|----------|------|
| V_{CC} | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V_{IH} | High-level input voltage | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | | V |
| V_{IL} | Low-level input voltage | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 0.8 | V |
| V_I | Input voltage | | 0 | 5.5 | V |
| V_O | Output voltage | High or low state | 0 | V_{CC} | V |
| | | 3 state | 0 | 5.5 | |
| I_{OH} | High-level output current | $V_{CC} = 2.7\text{ V}$ | | -12 | mA |
| | | $V_{CC} = 3\text{ V}$ | | -24 | |
| I_{OL} | Low-level output current | $V_{CC} = 2.7\text{ V}$ | | 12 | mA |
| | | $V_{CC} = 3\text{ V}$ | | 24 | |
| T_A | Operating free-air temperature | | -40 | 85 | °C |

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP† | MAX | UNIT |
|-----------------|---|----------------|--------------|------|----------|---------------|
| V_{OH} | $I_{OH} = -100\text{ }\mu\text{A}$ | 2.7 V to 3.6 V | $V_{CC}-0.2$ | | | V |
| | $I_{OH} = -12\text{ mA}$ | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| | $I_{OH} = -24\text{ mA}$ | 3 V | 2.2 | | | |
| V_{OL} | $I_{OL} = 100\text{ }\mu\text{A}$ | 2.7 V to 3.6 V | | | 0.2 | V |
| | $I_{OL} = 12\text{ mA}$ | 2.7 V | | | 0.4 | |
| | $I_{OL} = 24\text{ mA}$ | 3 V | | | 0.55 | |
| I_I | $V_I = 0\text{ to }5.5\text{ V}$ | 3.6 V | | | ± 5 | μA |
| I_{off} | $V_I\text{ or }V_O = 5.5\text{ V}$ | 0 | | | ± 10 | μA |
| I_{OZ} | $V_O = 0\text{ to }5.5\text{ V}$ | 3.6 V | | | ± 10 | μA |
| I_{CC} | $V_I = V_{CC}\text{ or GND}$ | 3.6 V | | | 10 | μA |
| | $3.6\text{ V} \leq V_I \leq 5.5\text{ V}^\ddagger$ | | | | 10 | |
| ΔI_{CC} | One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ | 2.7 V to 3.6 V | | | 500 | μA |
| C_i | $V_I = V_{CC}\text{ or GND}$ | 3.3 V | | 4 | | pF |
| C_o | $V_O = V_{CC}\text{ or GND}$ | 3.3 V | | 5.5 | | pF |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|----------------|-----------------|-------------|--|-----|-------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 1.5 | 4.9 | | 5.9 | ns |
| t_{en} | \overline{OE} | Y | 1.5 | 6.2 | | 7.6 | ns |
| t_{dis} | \overline{OE} | Y | 1.5 | 6.5 | | 7 | ns |
| $t_{sk(o)}^\S$ | | | | 1.2 | | | ns |

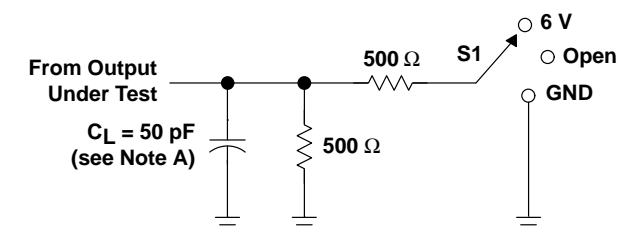
§ Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.



operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

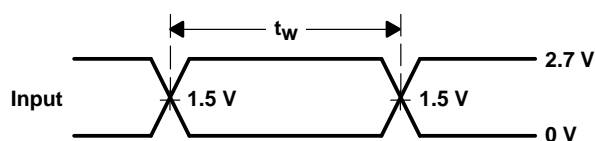
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|---|---------------------------------|-----|------|
| C_{pd} | Power dissipation capacitance per buffer/driver | $C_L = 0$, $f = 10\text{ MHz}$ | 44 | pF |
| | Outputs enabled | | 2 | |

PARAMETER MEASUREMENT INFORMATION

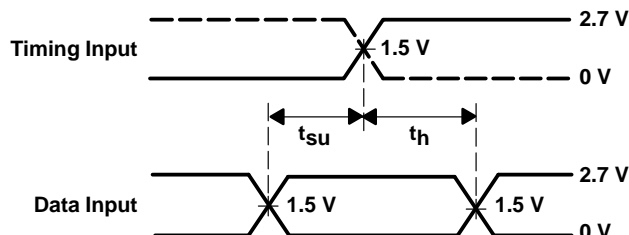


LOAD CIRCUIT

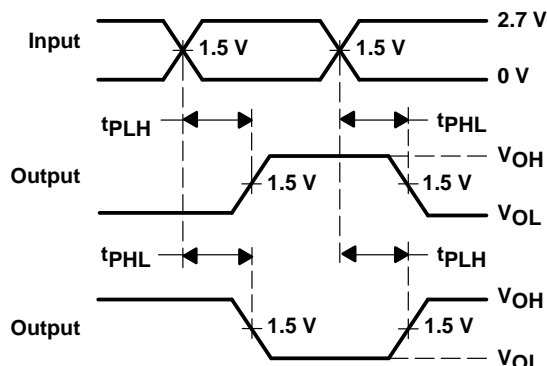
| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



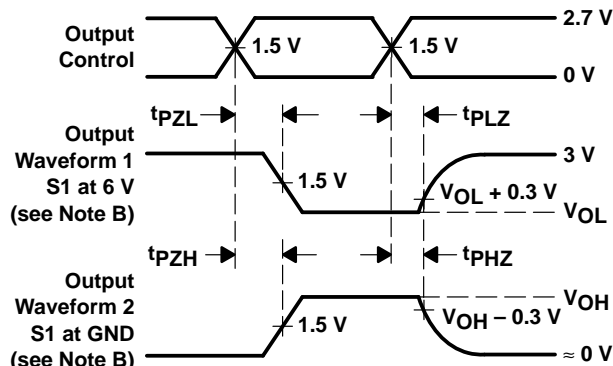
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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