

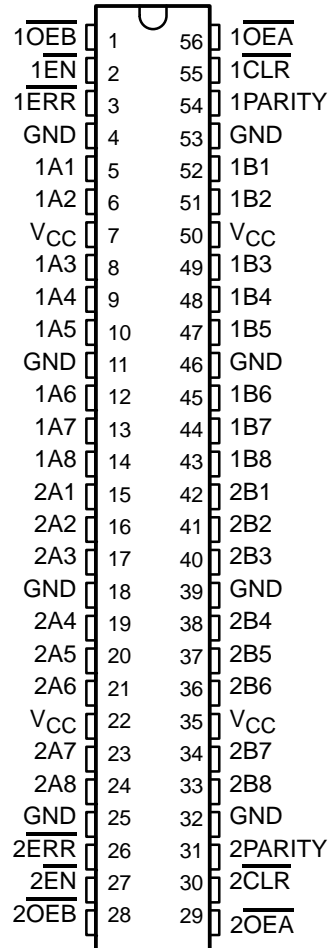
54AC16854, 54ACT16854
74AC16854, 74ACT16854
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCAS410 – JUNE 1990

- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

16854, 74ACT16854 . . . DL PACKAGE
 16854, 54ACT16854 . . . WD PACKAGE

(TOP VIEW)



description

The 'AC16854 and 'ACT16854 contain two inverting 8-bit-to-9-bit parity bus transceivers. For either transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output (1ERR̅ or 2ERR̅) is an open-collector output. 1ERR̅ (or 2ERR̅) can be passed, sampled, stored, and cleared from the latch using the latch enable (1EN̅ and 2EN̅) and clear (1CLR̅ and 2CLR̅) inputs.

The 74AC16854 and 74ACT16854 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16854 has CMOS-compatible input thresholds. The 'ACT16854 has TTL-compatible input thresholds.

The 54AC16854 and 54ACT16854 are characterized over the full military temperature range of –55°C to 125°C. The 74AC16854 and 74ACT16854 are characterized for operation from –40°C to 85°C.

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