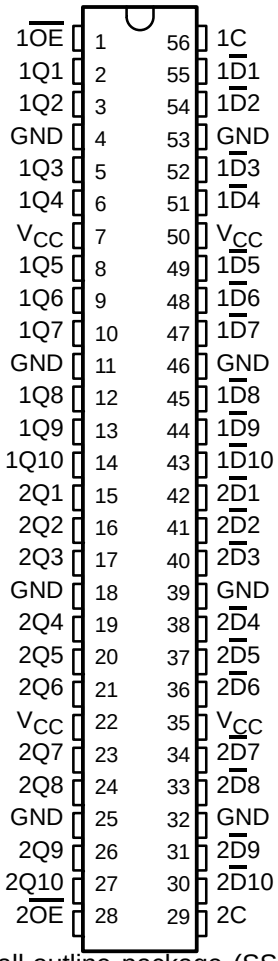
- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

l6842, 74ACT16842 . . . DL PACKAGE
l6842, 54ACT16842 . . . WD PACKAGE

(T0P VIEW)



description

The ’AC16842 and ’ACT16842 are inverting 20-bit D-type latches composed of two 10-bit sections with separate control signals. For each 10-bit section, when the enable input 1C (or 2C) is low, the latches are in the storage mode. In contrast, when 1C (or 2C) is high, the latches are transparent. In this mode, the inverse of the data present at the 1D (or 2D) inputs is transmitted to the 1Q (or 2Q) outputs if $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state.

The 74AC16842 and 74ACT16842 are packaged in TI’s shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The ’AC16842 has CMOS-compatible input thresholds. The ’ACT16842 has TTL-compatible input thresholds.

The 54AC16842 and 54ACT16842 are characterized over the full military temperature range of –55°C to 125°C. The 74AC16842 and 74ACT16842 are characterized for operation from –40°C to 85°C.

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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