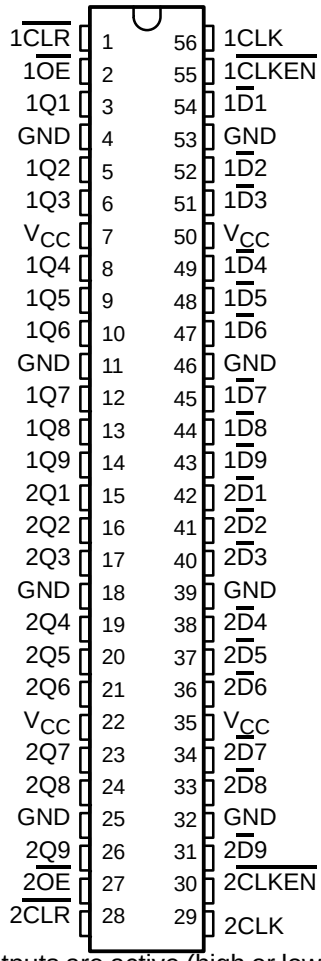
- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

74AC16824, 74ACT16824 . . . DL PACKAGE
74AC16824, 54ACT16824 . . . WD PACKAGE

(TOP VIEW)



description

The ’AC16824 and ’ACT16824 are inverting 18-bit D-type flip-flops composed of two 9-bit sections with separate control signals. For either 9-bit flip-flop section, if the clock enable (1$\overline{\text{CLKEN}}$ or 2$\overline{\text{CLKEN}}$) is low, the inverse of the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of 1CLK (or 2CLK). When 1$\overline{\text{CLKEN}}$ (or 2$\overline{\text{CLKEN}}$) is high, the flip-flops retain their previously stored values. Taking 1$\overline{\text{CLR}}$ (or 2$\overline{\text{CLR}}$)) low asynchronously clears the corresponding flip-flops.

When the output enable (1$\overline{\text{OE}}$ or 2$\overline{\text{OE}}$) is low, the corresponding Q outputs are active (high or low logic levels). When 1$\overline{\text{OE}}$ (or 2$\overline{\text{OE}}$) is high, the corresponding outputs are in the high-impedance state. 1$\overline{\text{OE}}$ (or 2$\overline{\text{OE}}$) does not affect the internal operation of the flip-flops: previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPUTS				FLIP-FLOP DATA	Q OUTPUTS
$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	$\overline{\text{OE}}$		
L	X	X	L	L	L
H	H	X	L	Previous $\overline{\text{D}}$ Data	Inverse of Previous $\overline{\text{D}}$ Data
H	X	L	L	Previous $\overline{\text{D}}$ Data	Inverse of Previous $\overline{\text{D}}$ Data
H	L	↑	L	Current $\overline{\text{D}}$ Data	Inverse of Current $\overline{\text{D}}$ Data
H	H	X	H	Previous $\overline{\text{D}}$ Data	Z
H	X	L	H	Previous $\overline{\text{D}}$ Data	Z
H	L	↑	H	Current $\overline{\text{D}}$ Data	Z

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PRODUCT PREVIEW

The 74AC16824 and 74ACT16824 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16824 has CMOS-compatible input thresholds. The 'ACT16824 has TTL-compatible input thresholds.

The 54AC16824 and 54ACT16824 are characterized over the full military temperature range of –55°C to 125°C. The 74AC16824 and 74ACT16824 are characterized for operation from –40°C to 85°C.

logic diagram (positive logic)

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