

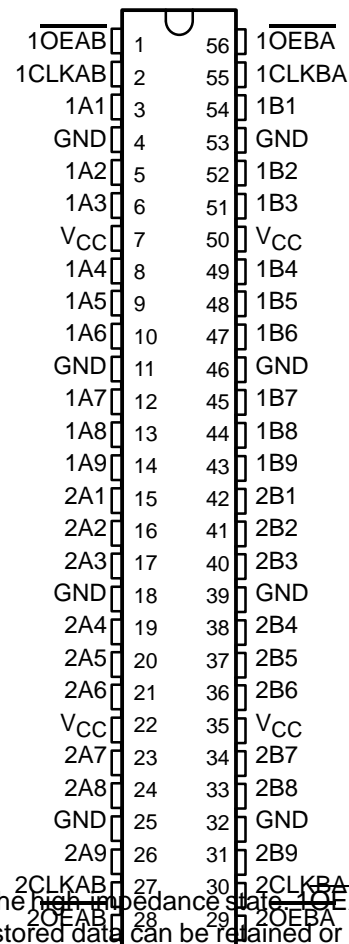
54AC16474, 74AC16474 18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS399A – JANUARY 1992

- Members of the Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Pin Spacings
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes Printed Circuit Board (PCB) Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

16474 . . . WD PACKAGE
16474 . . . DL PACKAGE

(TOP VIEW)



description

These devices are non-inverting 18-bit registered bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable ($\overline{1OEAB}$ or $\overline{2OEAB}$) and clock ($\overline{1CLKAB}$ or $\overline{2CLKAB}$) inputs. When $\overline{1OEAB}$ or $\overline{2OEAB}$ is low, the corresponding outputs are active (high or low) and take on either the current data on low-to-high transition of $\overline{1CLKAB}$ or $\overline{2CLKAB}$ or the previously stored data if $\overline{1CLKAB}$ or $\overline{2CLKAB}$ is low.

When $\overline{1OEAB}$ or $\overline{2OEAB}$ is high, the corresponding outputs are in the high-impedance state. $\overline{1OEAB}$ or $\overline{2OEAB}$ does not affect the operation on the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is similar, but uses $\overline{1OEBA}$ and/or $\overline{2OEBA}$ and $\overline{1CLKBA}$ and/or $\overline{2CLKBA}$.

The 74AC16474 is packaged in TI's shrink small-outline packages (DL) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same PCB area.

The 54AC16474 is characterized over the full military temperature range of -55°C to 125°C. The 74AC16474 is characterized for operation from -40°C to 85°C.

PRODUCT PREVIEW

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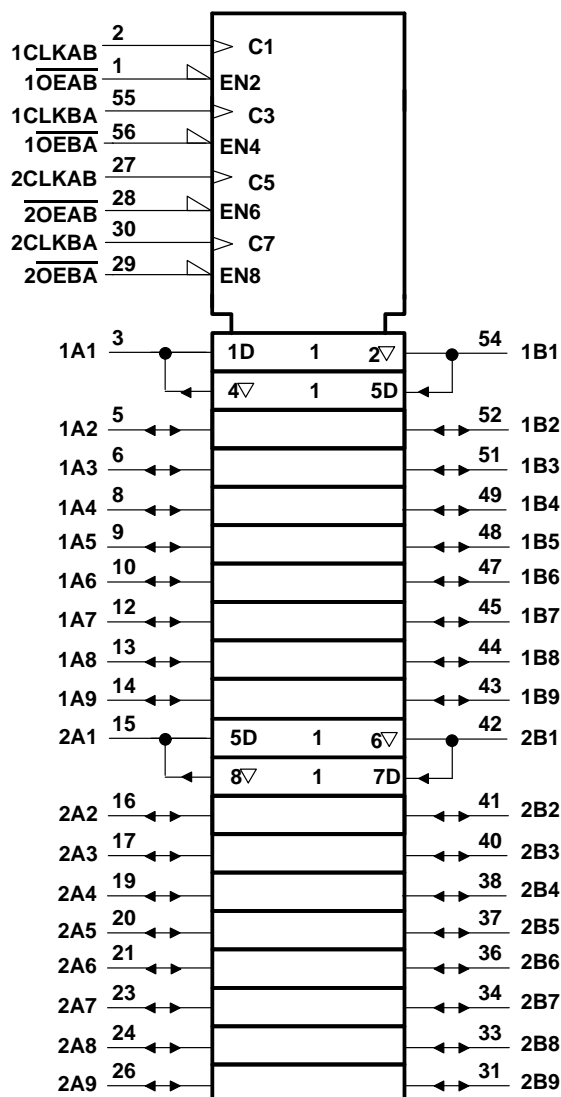
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INPUTS			OUTPUTS
CLKAB	OEAB	A	B
X	H	X	Z
L	L	X	B ₀ †
↑	L	H	H
↑	L	L	L

‡ Level of B before the indicated steady-state input conditions were established.

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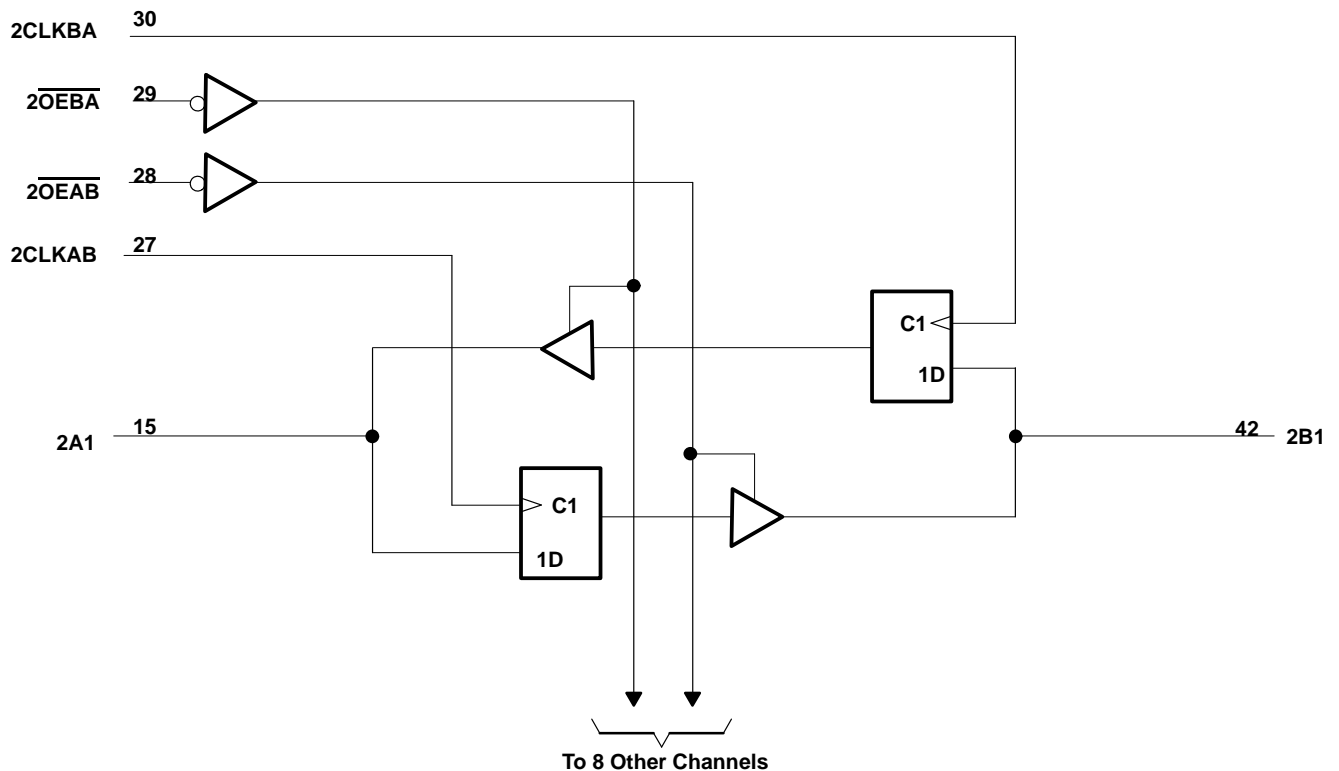
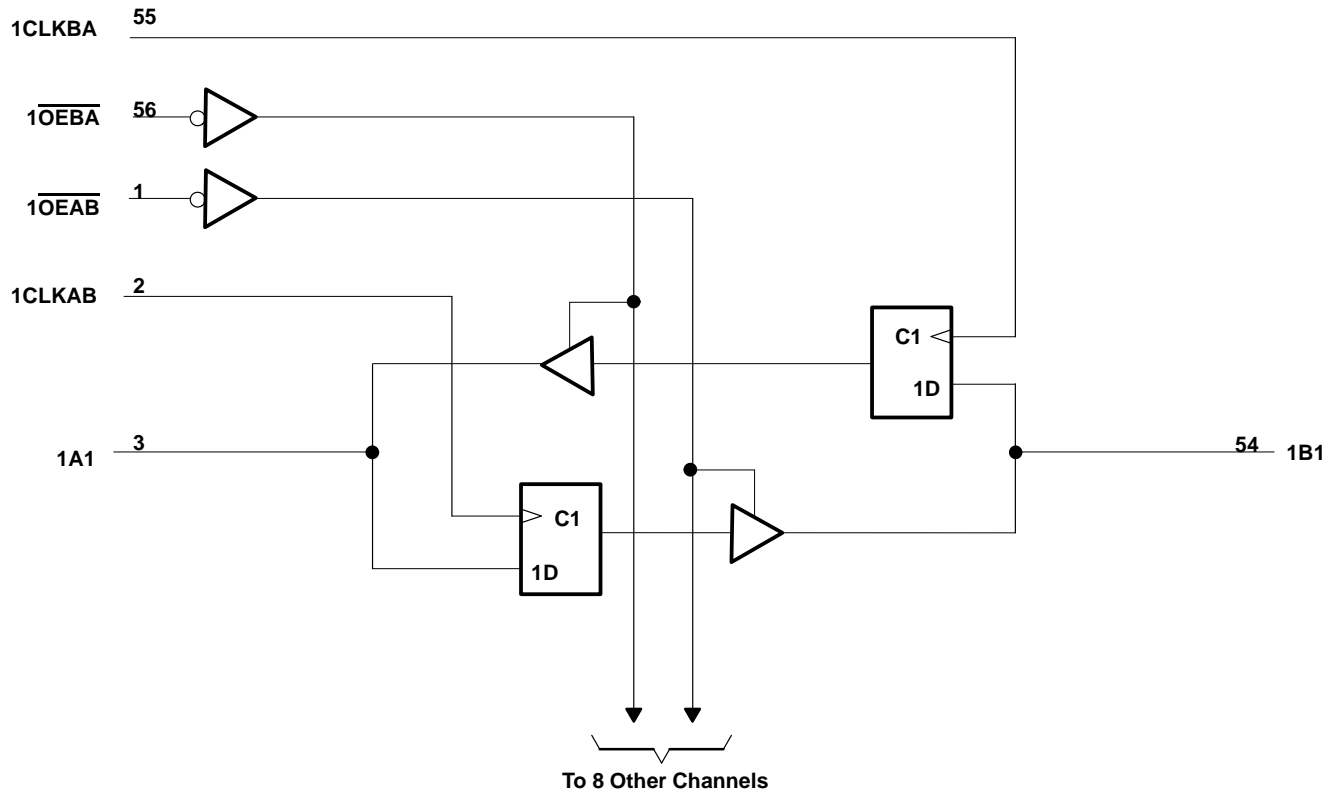


TEXAS
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54AC16474, 74AC16474 18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



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54AC16474, 74AC16474

18-BIT REGISTERED BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±450 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions (see Note 2)

			54AC16474			74AC16474			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V	0.9			0.9			V
		V _{CC} = 4.5 V	1.35			1.35			
		V _{CC} = 5.5 V	1.65			1.65			
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
I _{OH}	High-level output current	V _{CC} = 3 V	−4			−4			mA
		V _{CC} = 4.5 V	−24			−24			
		V _{CC} = 5.5 V	−24			−24			
I _{OL}	Low-level output current	V _{CC} = 3 V	12			12			mA
		V _{CC} = 4.5 V	24			24			
		V _{CC} = 5.5 V	24			24			
Δt/Δv	Input transition rise or fall rate		0	10		0	10		ns/V
T _A	Operating free-air temperature		−55	125		−40	85		°C

NOTE 2: Unused or floating (input or I/O) must be held high or low

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC16474		74AC16474		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	3 V	2.9			2.9		2.9		V	
		4.5 V	4.4			4.4		4.4			
		5.5 V	5.4			5.4		5.4			
	I _{OH} = –4 mA	3 V	2.58			2.4		2.48			
	I _{OH} = –24 mA	4.5 V	3.94			3.7		3.8			
		5.5 V	4.94			4.7		4.8			
	I _{OH} = –50 mA†	5.5 V				3.85					
I _{OH} = –75 mA†	5.5 V						3.85				
V _{OL}	I _{OL} = 50 μA	3 V	0.1			0.1		0.1		V	
		4.5 V	0.1			0.1		0.1			
		5.5 V	0.1			0.1		0.1			
	I _{OL} = 12 mA	3 V	0.36			0.5		0.44			
	I _{OL} = 24 mA	4.5 V	0.36			0.5		0.44			
		5.5 V	0.36			0.5		0.44			
	I _{OL} = 50 mA†	5.5 V				1.65					
I _{OL} = 75 mA†	5.5 V						1.65				
I _I	Control inputs	V _I = V _{CC} or GND	5.5 V	±0.1			±1		±1		μA
I _{OZ}	A or B ports‡	V _O = V _{CC} or GND	5.5 V	±0.5			±10		±5		μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V	8			160		80		μA
C _i	Control inputs	V _I = V _{CC} or GND	5 V	4.5							pF
C _{iO}	A or B ports	V _O = V _{CC} or GND	5 V	16							pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		T _A = 25°C		54AC16474		74AC16474		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency							MHz
t _{su}	Setup time, data before CLK↑							ns
t _h	Hold time, data after CLK↑							ns
t _w	Pulse duration	High						ns
		Low						

timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		T _A = 25°C		54AC16474		74AC16474		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency							MHz
t _{su}	Setup time, data before CLK↑							ns
t _h	Hold time, data after CLK↑							ns
t _w	Pulse duration	High						ns
		Low						

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC16474		74AC16474		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}										MHz
t_{PLH}	CLK	A or B								ns
t_{PHL}										
t_{PZH}	$\overline{\text{OE}}$	A or B								ns
t_{PZL}										
t_{PHZ}										
t_{PLZ}										

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

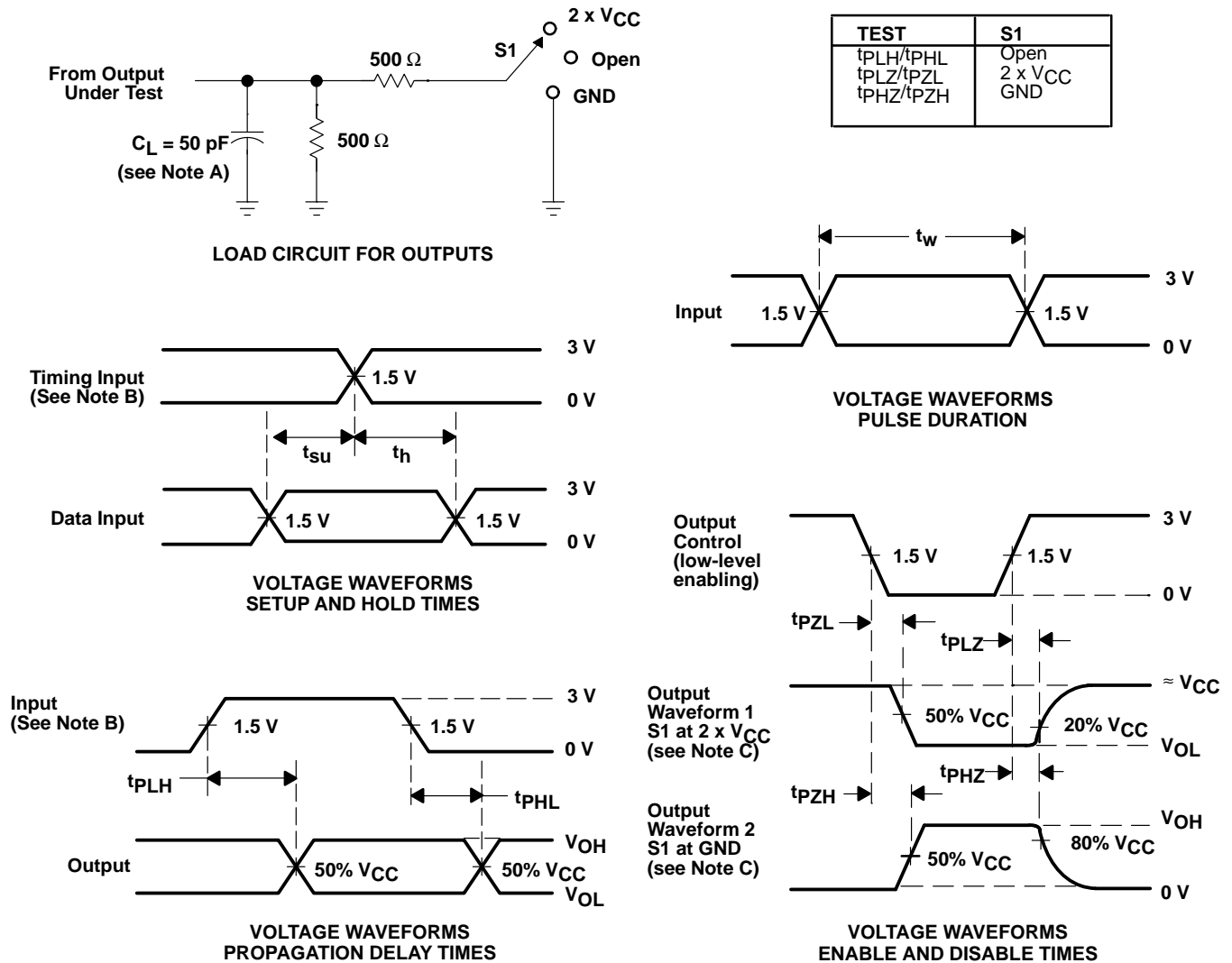
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC16474		74AC16474		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}										MHz
t_{PLH}	CLK	A or B								ns
t_{PHL}										
t_{PZH}	$\overline{\text{OE}}$	A or B								ns
t_{PZL}										
t_{PHZ}										
t_{PLZ}										

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$		pF
		Outputs disabled			

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns. For testing pulse duration: $t_r = t_f = 1$ to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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