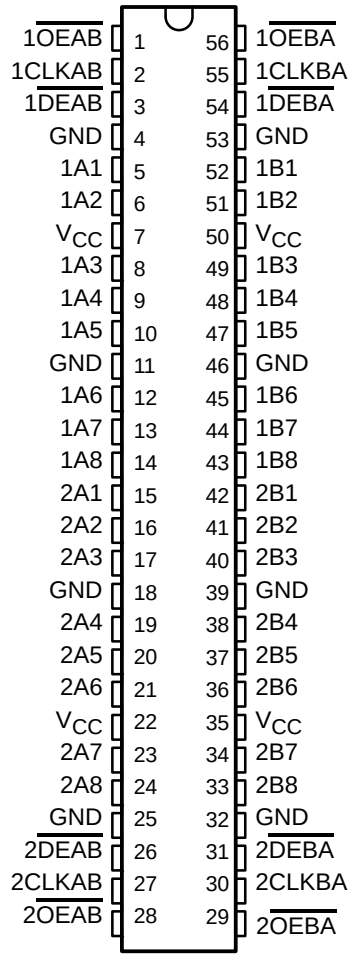
- **Members of Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

l6471, 74ACT16471 . . . DL PACKAGE
l6471, 54ACT16471 . . . WD PACKAGE

(T0P VIEW)



description

The ’AC16471 and ’ACT16471 are inverting 16-bit registered bus transceivers composed of two 8-bit sections with separate control signals. For either 8-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (1$\overline{OEAB}$ or 2$\overline{OEAB}$), direction-enable (1$\overline{DEAB}$ or 2$\overline{DEAB}$), and clock (1CLKAB or 2CLKAB) inputs.

When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is high, storage of the current A-bus data is inhibited and the corresponding B outputs are in the high-impedance state.When 1$\overline{DEAB}$ (or 2$\overline{DEAB}$) is low, the register contents and the output buffers are controlled by 1CLKAB (or 2CLKAB) and 1$\overline{OEAB}$ (or 2$\overline{OEAB}$). A low level on 1CLKAB (or 2 CLKAB) inhibits loading of the registers with the current A-bus data; a low-to-high transition on 1CLKAB (or 2CLKAB) causes the corresponding registers to be loaded with the current A-bus data. If 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) is low, the corresponding B outputs reflect the inverse of the register contents. A high level on 1$\overline{OEAB}$ (or 2$\overline{OEAB}$) causes the B outputs to be in the high-impedance state.

PRODUCT PREVIEW

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FUNCTION TABLE, EACH SECTION†

INPUTS			LATCH DATA	B OUTPUTS
DEAB	CLKAB	OEAB		
H	X	X	Previous A Data	Z
L	L	H	Previous A Data	Z
L	L	L	Previous A Data	Inverse of Previous A Data
L	↑	H	Current A Data	Z
L	↑	L	Current A Data	Inverse of Current A Data

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by $\overline{\text{DEBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

Data flow from B to A is similar, but uses 1$\overline{\text{OEBA}}$ and/or 2$\overline{\text{OEBA}}$, 1$\overline{\text{DEBA}}$ and/or 2$\overline{\text{DEBA}}$, and 1CLKBA and/or 2CLKBA.

The 74AC16471 and 74ACT16471 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16471 has CMOS-compatible input thresholds. The 'ACT16471 has TTL-compatible input thresholds.

The 54AC16471 and 54ACT16471 are characterized over the full military temperature range of –55°C to 125°C. The 74AC16471 and 74ACT16471 are characterized for operation from –40°C to 85°C.

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