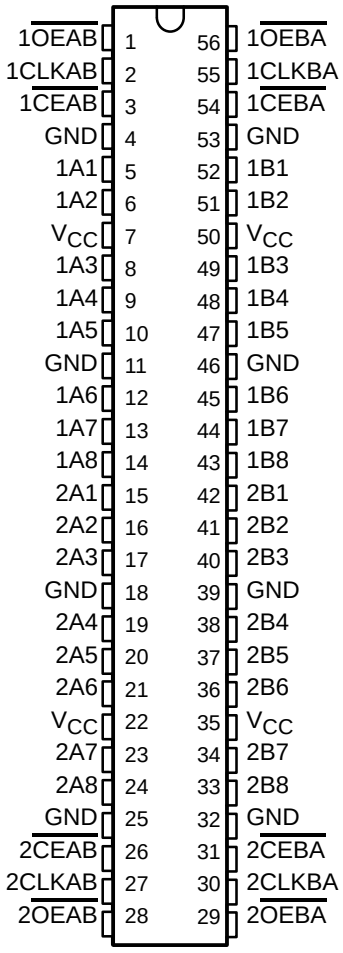
- **Members of the Texas Instruments Widebus™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Pin Spacings**
- **Flow-Through Architecture Optimizes Printed-Circuit-Board (PCB) Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

l6470 . . . WD PACKAGE
l6470 . . . DL PACKAGE

(T0P VIEW)



description

These devices are 16-bit registered transceivers that contain two sets of D-type flip-flops for temporary storage of data flowing in either direction. The device can be used as two 8-bit tranceivers or one 16-bit transceiver. Separate clock (CLKAB or CLKBA) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. If both $\overline{CEAB}$ and CLKAB are low, then B port will have the level of A port prior to the most recent low-to-high transition of CLKAB. Data flow from B to A is similar, but requires the use of $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$ inputs.

To avoid false clocking of the flip-flops, $\overline{CE}$ should not be switched from high to low while CLK is high.

The 74AC16470 is packaged in TI shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same PCB area.

The 54AC16470 is characterized over the full military temperature range of –55°C to 125°C. The 74AC16470 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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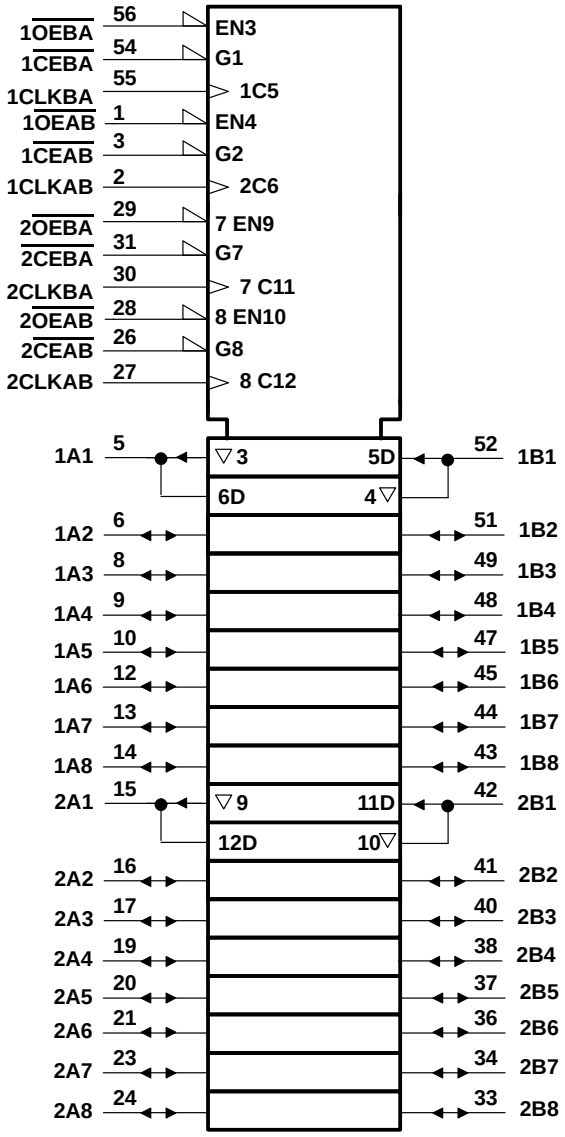
PRODUCT PREVIEW

FUNCTION TABLE

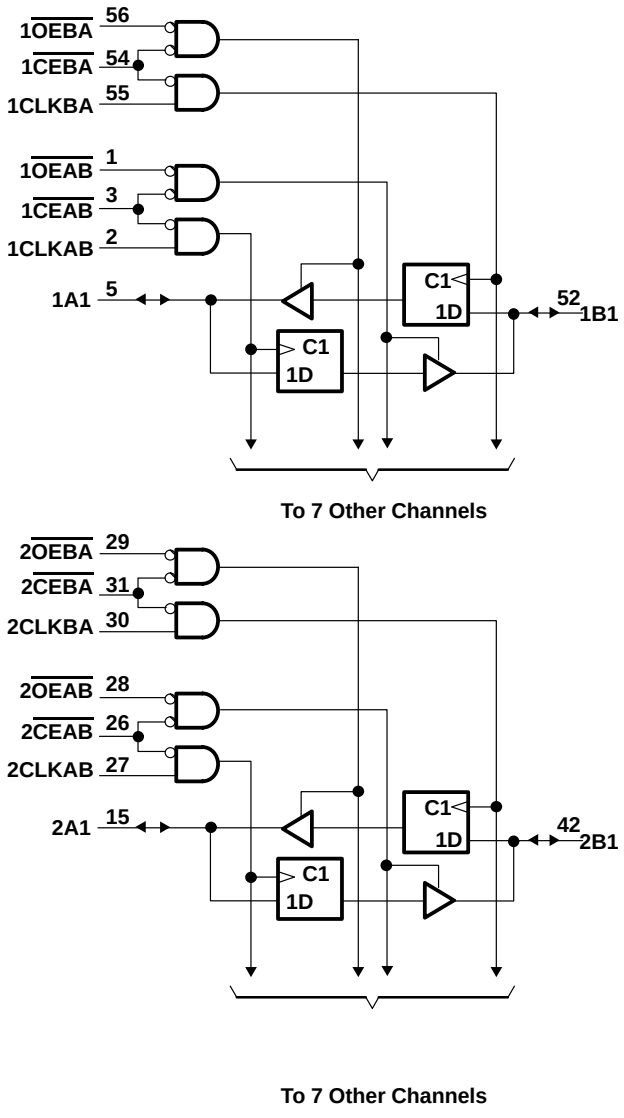
INPUTS				OUTPUT
CEAB	CLKAB	OEAB	A	B
H	X	X	X	Z
X	X	H	X	Z
L	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{CEBA}}$, CLKBA, and $\overline{\text{OEBA}}$.
‡ Output level before the indicated steady-state input conditions were established.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) . . . . . 1 W
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions (see Note 2)

			54AC16470			74AC16470			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: Unused or floating (input or I/O) must be held high or low

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16470		74AC16470		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 µA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = –4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = –24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = –50 mA†	5.5 V				3.85				
		I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V

PARAMETER			T_A = 25°C			54AC16470		74AC16470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency									MHz
t_w	Pulse duration	CLKAB or CLKBA high or low								ns
t_{su}	Setup time	Data before CLKAB or CLKBA↑								ns
		Data before $\overline{CEAB}$ or $\overline{CEBA}$↑								
t_h	Hold time	Data after CLKAB or CLKBA↑								ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑								

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V

PARAMETER			T_A = 25°C			54AC16470		74AC16470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency									MHz
t_w	Pulse duration	CLKAB or CLKBA high or low								ns
t_{su}	Setup time	Data before CLKAB or CLKBA↑								ns
		Data before $\overline{CEAB}$ or $\overline{CEBA}$↑								
t_h	Hold time	Data after CLKAB or CLKBA↑								ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑								

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16470		74AC16470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax										MHz
t_{PLH}	CLK	A or B								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	A or B								ns
t_{PLZ}										
t_{PZH}	$\overline{CE}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{CE}$	A or B								ns
t_{PLZ}										

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V

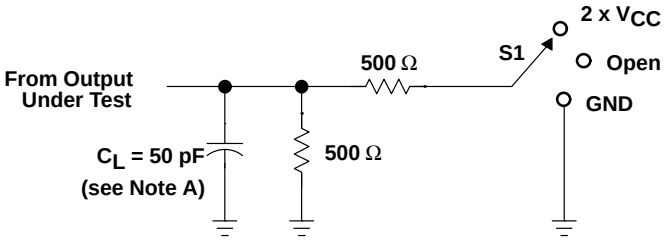
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16470		74AC16470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax										MHz
t_{PLH}	CLK	A or B								ns
t_{PHL}										
t_{PZH}	$\overline{OE}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{OE}$	A or B								ns
t_{PLZ}										
t_{PZH}	$\overline{CE}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{CE}$	A or B								ns
t_{PLZ}										

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz		pF
		Outputs disabled				

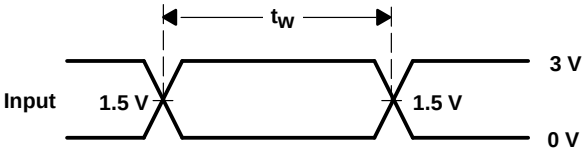
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

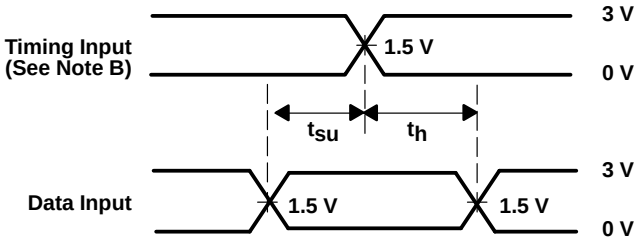


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

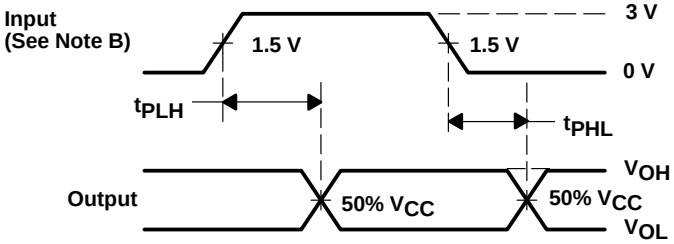
LOAD CIRCUIT FOR OUTPUTS



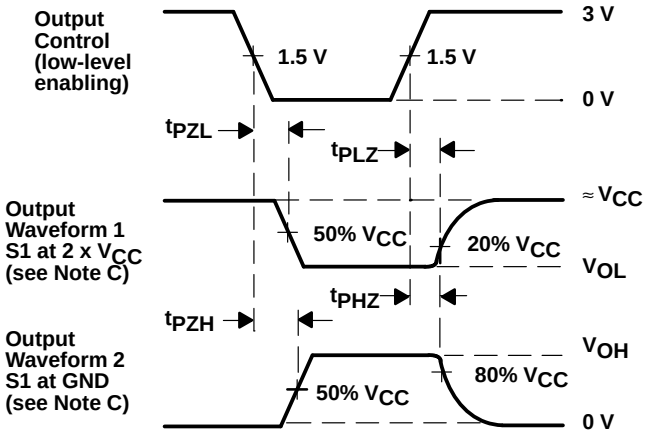
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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