

54AC16241, 74AC16241 16-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCAS394 – JANUARY 1992

- Member of the Texas Instruments Widebus™ Family
- Packaged in Shrink Small Outline 300-mil Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Pin Spacings
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes Printed-Circuit-Board (PCB) Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

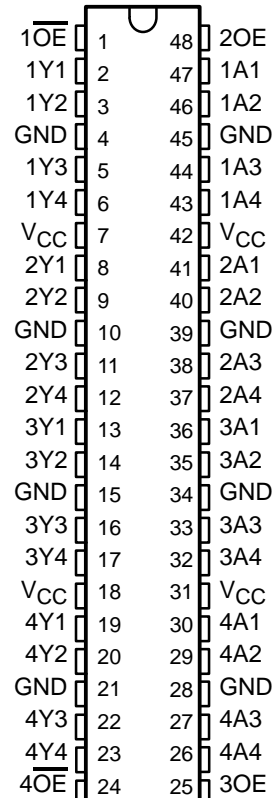
The 54AC16241 and 74AC16241 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and complementary OE and $\overline{\text{OE}}$ output-enable inputs.

The 'AC16241 is packaged in the TI's shrink small-outline package (DL), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16241 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16241 is characterized for operation from –40°C to 85°C.

I6241 ... WD PACKAGE
I6241 ... DL PACKAGE

(TOP VIEW)



FUNCTION TABLES

INPUTS		OUTPUT Y
$\overline{\text{OE}}$	A	
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

**TEXAS
INSTRUMENTS**
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

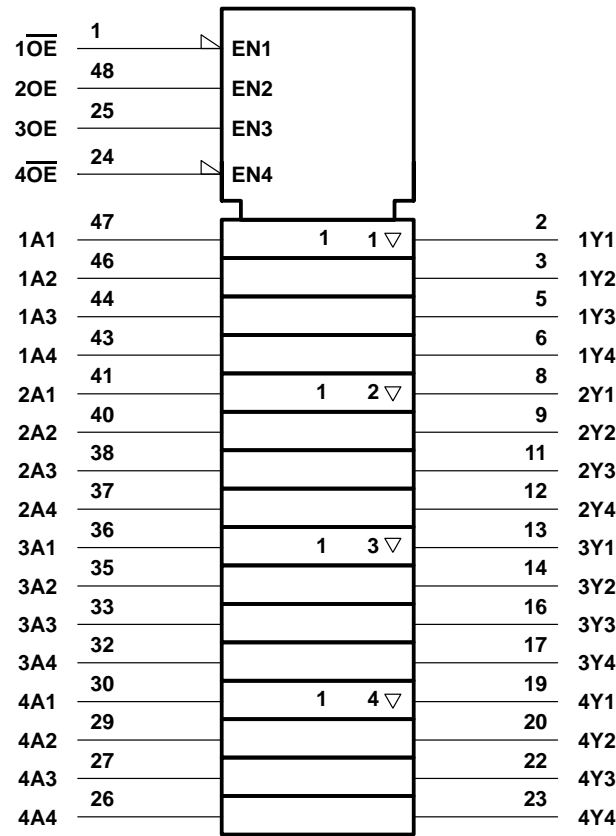
Copyright © 1991, Texas Instruments Incorporated

PRODUCT PREVIEW

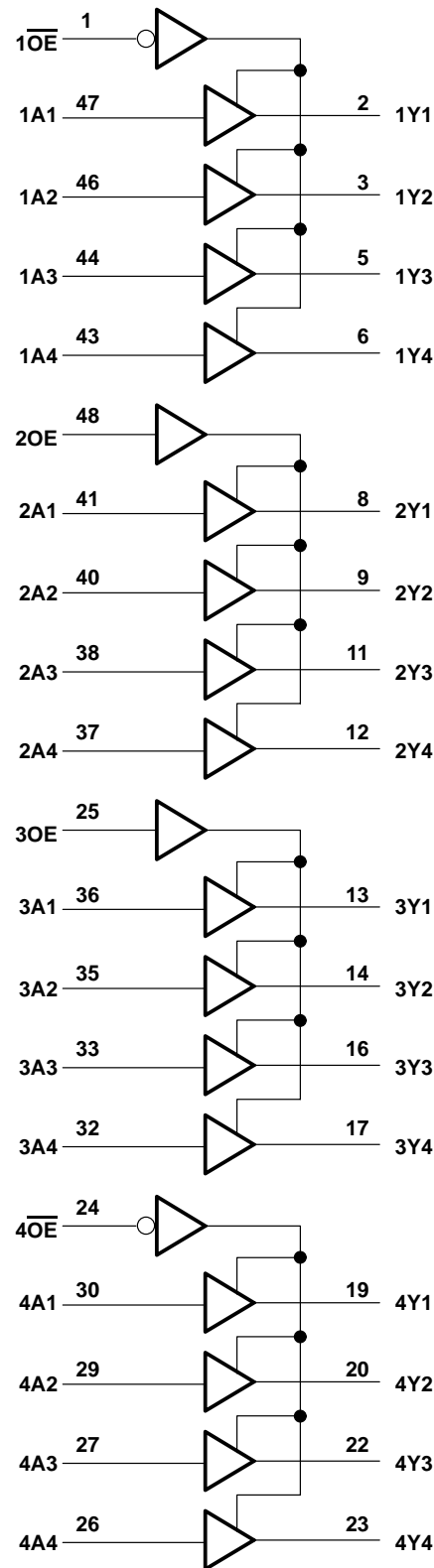
54AC16241, 74AC16241
 16-BIT BUFFERS AND LINE DRIVERS
 WITH 3-STATE OUTPUTS

DXXXX, JANUARY 1992

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

54AC16241, 74AC16241
16-BIT BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

DXXXX, JANUARY 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 400 mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air)	0.85 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions (see Note 2)

			54AC16241			74AC16241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V	0.9			0.9			V
		V _{CC} = 4.5 V	1.35			1.35			
		V _{CC} = 5.5 V	1.65			1.65			
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
I _{OH}	High-level output current	V _{CC} = 3 V	−4			−4			mA
		V _{CC} = 4.5 V	−24			−24			
		V _{CC} = 5.5 V	−24			−24			
I _{OL}	Low-level output current	V _{CC} = 3 V	12			12			mA
		V _{CC} = 4.5 V	24			24			
		V _{CC} = 5.5 V	24			24			
Δt/Δv	Input transition rise or fall rate		0	10		0	10		ns/V
T _A	Operating free-air temperature		−55	125		−40	85		°C

NOTE 2: Unused or floating (input or I/O) must be held high or low

PRODUCT PREVIEW

54AC16241, 74AC16241

16-BIT BUFFERS AND LINE DRIVERS

WITH 3-STATE OUTPUTS

DXXXX, JANUARY 1992

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC16241		74AC16241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		5.5 V				1.65				
I _{OH}	I _{OH} = -50 mA†	5.5 V								µA
		5.5 V								
I _{OL}	I _{OL} = 75 mA†	5.5 V								µA
		5.5 V								
I _I	Control inputs	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1	µA
I _{OZ}	A or B ports‡	V _O = V _{CC} or GND	5.5 V		±0.5		±10		±5	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V		8		160		80	µA
C _i	Control inputs	V _I = V _{CC} or GND	5 V		4.5					pF
C _{io}	A or B ports	V _O = V _{CC} or GND	5 V		16					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16241		74AC16241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y								ns
t _{PHL}										
t _{PZH}	$\overline{\text{OE}}$ or OE	Y								ns
t _{PZL}										
t _{PHZ}	$\overline{\text{OE}}$ or OE	Y								ns
t _{PLZ}										

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16241		74AC16241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y								ns
t _{PHL}										
t _{PZH}	$\overline{\text{OE}}$ or OE	Y								ns
t _{PZL}										
t _{PHZ}	$\overline{\text{OE}}$ or OE	Y								ns
t _{PLZ}										

54AC16241, 74AC16241
16-BIT BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

DXXXX, JANUARY 1992

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$)

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled		pF
		Outputs disabled		

C_L = 50 pF, f = 1 MHz

PRODUCT PREVIEW

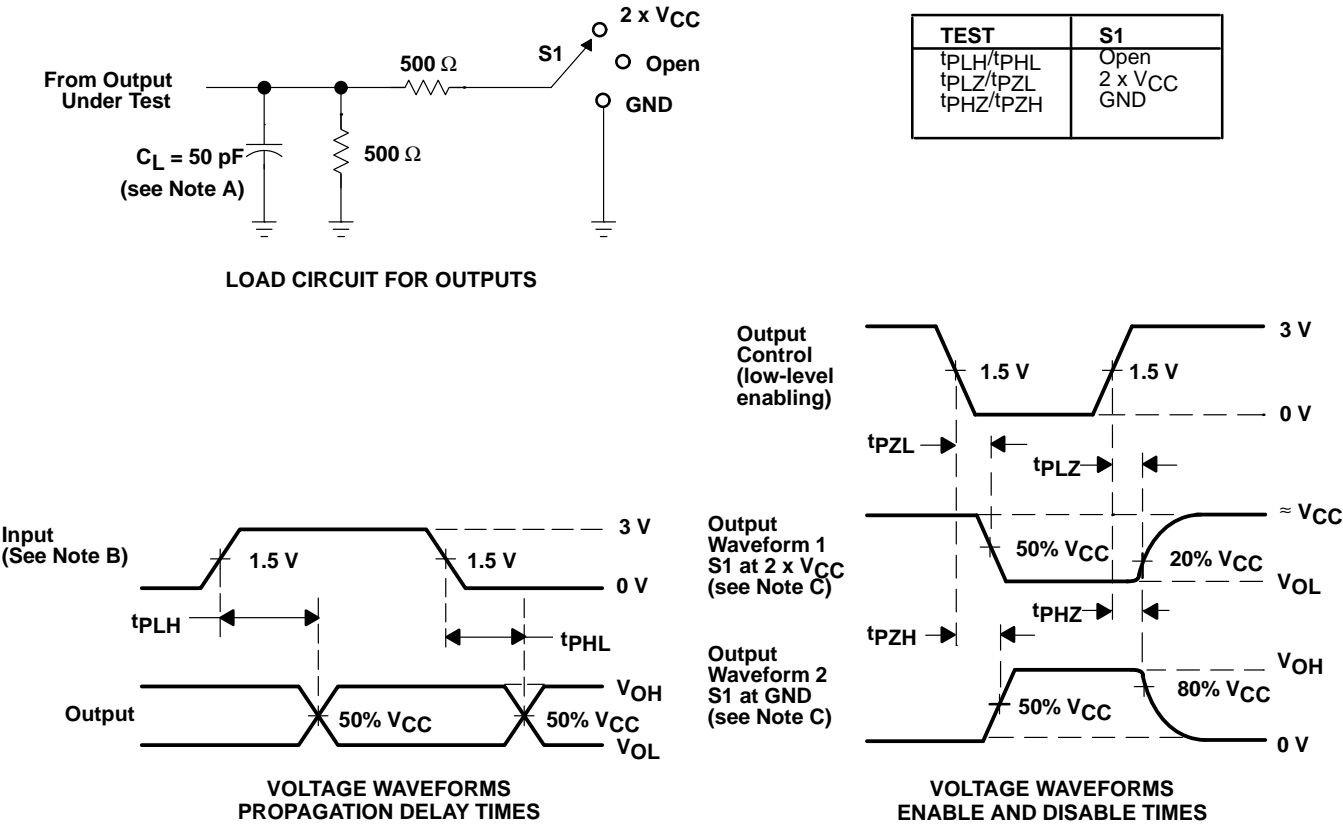
54AC16241, 74AC16241

16-BIT BUFFERS AND LINE DRIVERS

WITH 3-STATE OUTPUTS

DXXXX, JANUARY 1992

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. CL includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, tr ≤ 3 ns, tf ≤ 3 ns. For testing pulse duration: tr = tf = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.