- **Latchable P Input ports with Power-Up Clear**
- **Choice of Logical or Arithmetic (2's Complement) Comparison**
- **Data and PLE Inputs Utilize P-N-P Input Transistors to Reduce DC Loading Effects**
- **Approximately 35% Improvement in AC Performance Over Schottky TTL while Performing More Functions**
- **Cascadable to n-Bits while Maintaining High Performance**
- **10% Less Power than STTL for an 8-Bit Comparison**
- **Inputs are TTL-Voltage Compatible**
- **New flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two full decoded decisions about words P and Q are externally available at two outputs. These devices are full expandable to any number of bits without external gates. The P > Q and P < Q outputs of a stage handling less-significant bits may be connected to the P > Q and P < Q inputs of the next stage handling more-significant bits to obtain comparisons of words of longer lengths. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in the typical application data.

The latch is transparent when P Latch Enable (PLE) is high; the P input port is latched when PLE is low. This provides the designer with temporary storage for the P data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE and P and Q data inputs utilize p-n-p input transistors to reduce the low-level current input requirements to typically – 0.25 mA, which minimizes dc loading effects.

The 54ACT11885 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11885 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

COMPARISON	$\overline{L}/A$	DATA INPUTS	INPUTS		OUTPUTS	
		P0-P7, Q0-Q7	P>Q	P<Q	P>Q	P<Q
LOGICAL	H	P>Q	X	X	H	L
LOGICAL	H	P<Q	X	X	L	H
LOGICAL†	H	P=Q	H OR L	H OR L	H OR L	H OR L
ARITHMETIC	L	P AG Q	X	X	H	L
ARITHMETIC	L	Q AG P	X	X	L	H
ARITHMETIC	L	P=Q	H OR L	H OR L	H OR L	H OR L

† In these cases the P>Q output will follow the P>Q input, and the P<Q output will follow the P<Q input.

NOTE 1: AG-–arithmetically greater than

logic symbol‡

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input diode current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output diode current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND pins . . . . . ± 200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11885		74ACT11885		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	− 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11885		74ACT11885		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	mA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_I	$V_I = V_{CC}$ or GND	5 V		3.5						pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11885		74ACT11885		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	LA	P<Q, P>Q								ns
t_{PHL}	LA	P<Q, P>Q								ns
t_{PLH}	P<Q_{in}	P<Q, P>Q								ns
t_{PHL}	P<Q_{in}	P<Q, P>Q								ns
t_{PLH}	Any P or Q Data Input	P<Q, P>Q								ns
t_{PHL}	Any P or Q Data Input	P<Q, P>Q								ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz		pF
	Outputs disabled	C_L = 50 pF, f = 1 MHz		pF

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