- **Capable of Anticipating the Carry Across a Group of Eight 4-Bit Binary Adders**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Typical Carry Time, C_n to Any C_{n+i}, is Less Than 6 ns**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

The ACT11882 is a high-speed look-ahead carry generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'T11882's full look-ahead is possible across n-bit adders.

The SN54ACT11882 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT11882 is characterized for operation from – 40°C to 85°C.

'11882 LOGIC EQUATIONS

$$C_{n+8} = G1+P1G0+P1P0C_n$$

$$C_{n+16} = G3+P3G2+P3P2G1+P3P2P1G0 + P3P2P1P0C_n$$

$$C_{n+24} = G5+P5G4+P5P4G3+P5P4P3G2 + P5P4P3P2G1+P5P4P3P2P1G0 + P5P4P3P2P1P0C_n$$

$$C_{n+32} = G7+P7G6+P7P6G5+P7P6P5G4 + P7P6P5P4G3+P7P6P5P4P3G2 + P7P6P5P4P3P2G1+P7P6P5P4P3P2P1G0 + P7P6P5P4P3P2P1P0C_n$$

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FUNCTION TABLE FOR C_{n+32} OUTPUT

INPUTS																	OUTPUT
$\overline{G7}$	$\overline{G6}$	$\overline{G5}$	$\overline{G4}$	$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P7}$	$\overline{P6}$	$\overline{P5}$	$\overline{P4}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+32}
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

FUNCTION TABLE FOR C_{n+24} OUTPUT

INPUTS													OUTPUT
$\overline{G5}$	$\overline{G4}$	$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P5}$	$\overline{P4}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+24}
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

FUNCTION TABLE FOR C_{n+16} OUTPUT

INPUTS									OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+16}
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	L	H
All other combinations									L

FUNCTION TABLE FOR C_{n+8} OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+8}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input diode current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output diode current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND pins . . . . . ± 100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11882		74ACT11882		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	− 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11882		74ACT11882		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	mA
ΔI_{CC}‡	$V_I = V_{CC}$ or GND	5.5 V			0.9		1		1	mA
C_I	$V_I = V_{CC}$ or GND	5 V		4.5						pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V TO 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			54ACT11882		74ACT11882		
			MIN	MAX	MIN	MAX	
t_{PLH}	C_n	Any output					ns
t_{PHL}							
t_{PLH}	P or G	C_{n+8}					ns
t_{PHL}							
t_{PLH}	P or G	C_{n+16}					ns
t_{PHL}							
t_{PLH}	P or G	C_{n+24}					ns
t_{PHL}							
t_{PLH}	P or G	C_{n+32}					ns
t_{PHL}							

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