- **Inputs are TTL-Voltage Compatible**
- **Full Look-Ahead for High-Speed Operations on Long Words**
- **Arithmetic Operating Modes: Addition, Subtraction, Shift Operand A One Position, Magnitude Comparison, Plus Twelve Other Arithmetic Operations**
- **Logic Function Modes Exclusive-OR, Comparator, AND, NAND, OR, NOR, Plus Ten Other Logic Operations**
- **Provides Status Register Checks**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

logic symbol†

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signal designations

In both Figures 1 and 2, the polarity indicators (◺) indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figures 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.

PIN numbers shown are for DW, JT, and NT packages.

description

The ’ACT11881 arithmetic logic unit (ALU)/function generators have a complexity of 77 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, $\overline{G}$ and $\overline{P}$, for the four bits in the package. When used in conjunction with the 54ACT11882 or 74ACT11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading ’ACT11882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The ’ACT11881 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-low data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	C_n	$\overline{C_{n+4}}$	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C_n}$	C_{n+4}	X	Y

Subtraction is accomplished by 1’s complement addition, where the 1’s complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The ’ACT11881 can also be used as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with C_n=H when performing this comparison. The A=B output is open-collector so that it can be wired-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer’s requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

The ’ACT11881 has the same pinout and same functionality as the ’ACT11181 except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

Table 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = A + $\overline{B}$ PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Table 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND pins . . . . . ± 200 mA
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11881		74ACT11881		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11881		74ACT11881		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	A = B	$V_O = V_{CC}$	5.5 V			0.5		10		5	μA
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I		$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡		$V_I = V_{CC}$ or GND	5.5 V			0.9		1		1	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	A = B	$V_O = V_{CC}$ or GND	5 V		11						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

SUM mode; M = S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11881		74ACT11881		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}								ns
t_{PHL}										
t_{PLH}	Any Ai	C_{n+4}								ns
t_{PHL}										
t_{PLH}	Any Bi	C_{n+4}								ns
t_{PHL}										
t_{PLH}	C_n	Any F								ns
t_{PHL}										
t_{PLH}	Any A	G								ns
t_{PHL}										
t_{PLH}	Any B	G								ns
t_{PHL}										
t_{PLH}	Any A	P								ns
t_{PHL}										
t_{PLH}	Any B	P								ns
t_{PHL}										
t_{PLH}	Ai	Fi								ns
t_{PHL}										
t_{PLH}	Bi	Fi								ns
t_{PHL}										
t_{PLH}	Any A	Any Fi								ns
t_{PHL}										
t_{PLH}	Any Bi	Any Fi								ns
t_{PHL}										
t_{PLH}	M	Any F								ns
t_{PHL}										
t_{PLH}	M	A = B								ns
t_{PHL}										

NOTE 2: Load circuits and voltage waveforms are shown in Section 1 of *Advanced CMOS Logic Data Book*, 1990.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

DIFF mode; M = S0 = S3 = 0 V, S1 = S2 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11881		74ACT11881		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}								ns
t_{PHL}										
t_{PLH}	Any Ai	C_{n+4}								ns
t_{PHL}										
t_{PLH}	Any Bi	C_{n+4}								ns
t_{PHL}										
t_{PLH}	Any A	G								ns
t_{PHL}										
t_{PLH}	C_n	Any F								ns
t_{PHL}										
t_{PLH}	Any B	G								ns
t_{PHL}										
t_{PLH}	Any A	P								ns
t_{PHL}										
t_{PLH}	Any B	P								ns
t_{PHL}										
t_{PLH}	Ai	Fi								ns
t_{PHL}										
t_{PLH}	Bi	Fi								ns
t_{PHL}										
t_{PLH}	Any A	Any Fi								ns
t_{PHL}										
t_{PLH}	Any Bi	Any Fi								ns
t_{PHL}										
t_{PLH}	Any A	A = B								ns
t_{PHL}										
t_{PLH}	Any B	A = B								ns
t_{PHL}										

NOTE 2:Load circuits and voltage waveforms are shown in Section 1 of *Advanced CMOS Logic Data Book*, 1990.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

LOGIC and $\overline{\text{ARITH}}$ MODES

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			54ACT11881		74ACT11881		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Ai	Any Fi	M = 4.5 V (LOGIC mode)								ns
t_{PHL}											
t_{PLH}	Bi	Fi	M = 4.5 V (LOGIC mode)								ns
t_{PHL}											
t_{PLH}	Any S	Any F	M = 0 V ($\overline{\text{ARITH}}$ mode)								ns
t_{PHL}											
t_{PLH}	Any S	A = B	M = 0 V ($\overline{\text{ARITH}}$ mode)								ns
t_{PHL}											
t_{PLH}	Any S	C_{n+4}	M = 4.5 V (LOGIC mode)								ns
t_{PHL}											
t_{PLH}	Any S	G	M = 0 V ($\overline{\text{ARITH}}$ mode)								ns
t_{PHL}											
t_{PLH}	Any S	P	M = 4.5 V (LOGIC mode)								ns
t_{PHL}											

switching characteristics involving status checks, V_{CC} = 5 V ± 0.5 V, C_n = 4.5 V, M = 4.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			54ACT11881		74ACT11881		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any A or B	P	S0=S3=4.5 V, S1=S2=0 V, ($\overline{A}$i=$\overline{B}$i or $\overline{A}$i≠$\overline{B}$i)								ns
t_{pd}	Any A or B	C_{n+4}	S0=S3=4.5 V, S1=S2=0 V, ($\overline{A}$i=$\overline{B}$i or $\overline{A}$i≠$\overline{B}$i)								ns
t_{pd}	Any A or B	P	S2=4.5 V, S0=S1=S3=0 V, ($\overline{A}$i=$\overline{B}$i=H or L)								ns
t_{pd}	Any A or B	P	S2=4.5 V, S0=S1=S3=0 V, ($\overline{A}$i=$\overline{B}$i=H or L)								ns

NOTE 2:Load circuits and voltage waveforms are shown in Section 1 of *Advanced CMOS Logic Data Book*, 1990.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	170	pF

PARAMETER MEASUREMENT INFORMATION

SUM Mode Test Table

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	In-Phase

PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase

PARAMETER MEASUREMENT INFORMATION

Logic Mode Test Table

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$, and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

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