SN74ALVC162601
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCAS376 – MARCH 1994

- **Member of the Texas Instruments** *Widebus*™ **Family**
- *UBT*™ **(Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- *EPIC*™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on All I/O Pins**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{\text{OEAB}}$	1	56	$\overline{\text{CLKENAB}}$
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
$\overline{\text{OEBA}}$	27	30	CLKBA
LEBA	28	29	$\overline{\text{CLKENBA}}$

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable $\overline{\text{OEAB}}$ is active low. When $\overline{\text{OEAB}}$ is low, the outputs are active. When $\overline{\text{OEAB}}$ is high, the outputs are in the high-impedance state.
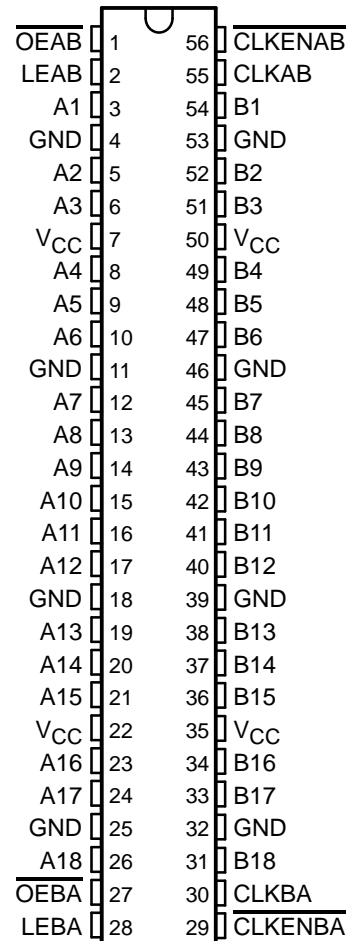
Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

The B-port outputs, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74ALVC162601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC162601 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE[†]

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0[‡]
H	L	L	X	X	B_0[‡]
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0[‡]
L	L	L	H	X	B_0[§]

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

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logic diagram (positive logic)

To 17 Other Channels

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package .... 1 W
                                                                                   DL package .... 1.4 W
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
         2. This value is limited to 4.6 V maximum.
         3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
             For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V			mA
		V_{CC} = 3 V			
I_{OL}	Low-level output current	V_{CC} = 2.7 V			mA
		V_{CC} = 3 V			
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$		MIN to MAX	$V_{CC}-0.2$	V
		$I_{OH} = -4\ mA$		2.7 V	2.4	
		$I_{OH} = -6\ mA$		3 V	2.4	
		$I_{OH} = TBD$			2	
V_{OL}		$I_{OL} = 100\ \mu A$		MIN to MAX	0.2	V
		$I_{OL} = 4\ mA$		2.7 V	0.4	
		$I_{OL} = 6\ mA$		3 V	0.4	
		$I_{OH} = TBD$			0.8	
I_I		$V_I = V_{CC}$ or GND		3.6 V	±5	μA
$I_{I(hold)}$		$V_I = 0.8\ V$		3 V	75	μA
		$V_I = 2\ V$			−75	
I_{OZ}‡		$V_O = V_{CC}$ or GND		3.6 V	±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6 V	40	μA
ΔI_{CC}		$V_{CC} = 3\ V$ to 3.6 V,	One input at $V_{CC} - 0.6\ V$,		750	μA
		Other inputs at V_{CC} or GND				
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

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