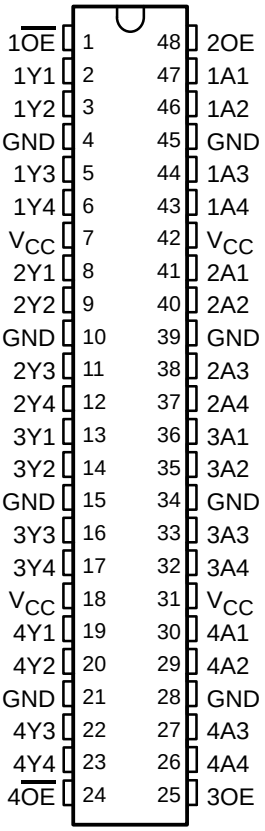
- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCH16241A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

This device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer, and provides true outputs and complementary output-enable (OE and $\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16241A is characterized for operation from –40°C to 85°C.

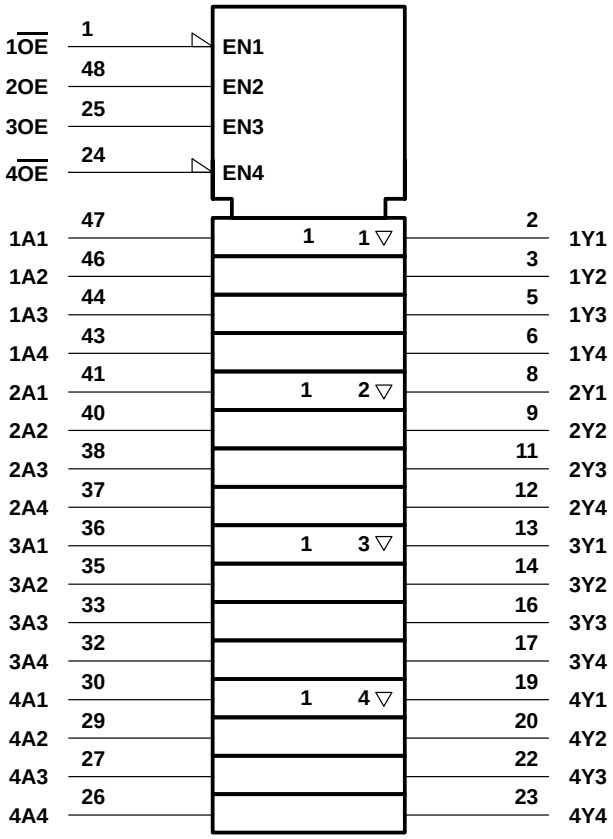
PRODUCT PREVIEW

FUNCTION TABLES

INPUTS		OUTPUTS
$1\overline{OE}$, $4\overline{OE}$	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUTS
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

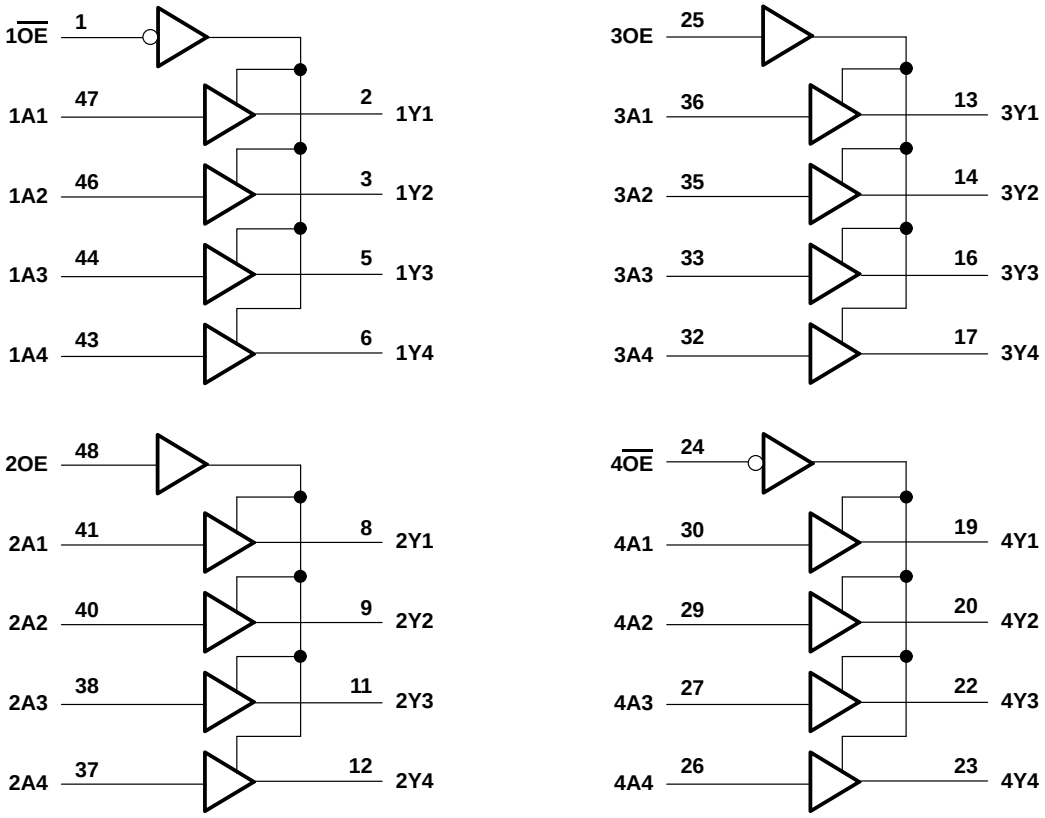
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O
(see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) (see Note 2) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3 state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	I_{OH} = –100 μA		2.7 V to 3.6 V	V_{CC}–0.2			V
	I_{OH} = –12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = –24 mA		3 V	2.2			
V_{OL}	I_{OL} = 100 μA		2.7 V to 3.6 V			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±5	μA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75			μA
	V_I = 2 V		3 V	–75			
	V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{off}	V_I or V_O = 5.5 V		0			±10	μA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±10	μA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			10	μA
	3.6 V ≤ V_I ≤ 5.5 V§					10	
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C_i	V_I = V_{CC} or GND		3.3 V				pF
C_o	V_O = V_{CC} or GND		3.3 V				pF

† All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ This applies in the disabled state only.

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