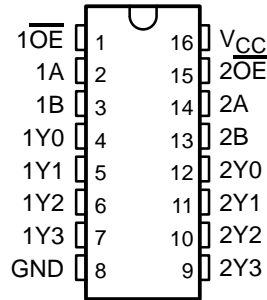# SN74LVC139A
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS341C – MARCH 1994 – REVISED JANUARY 1997

- *EPIC*™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	16	V_{CC}
1A	2	15	2$\overline{OE}$
1B	3	14	2A
1Y0	4	13	2B
1Y1	5	12	2Y0
1Y2	6	11	2Y1
1Y3	7	10	2Y2
GND	8	9	2Y3

description

This dual 2-line to 4-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC139A is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The device comprises two individual 2-line to 4-line decoders in a single package. The active-low output-enable ($\overline{OE}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC139A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{OE}$	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

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PRODUCT PREVIEW

SN74LVC139A
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

logic symbols (alternatives)†
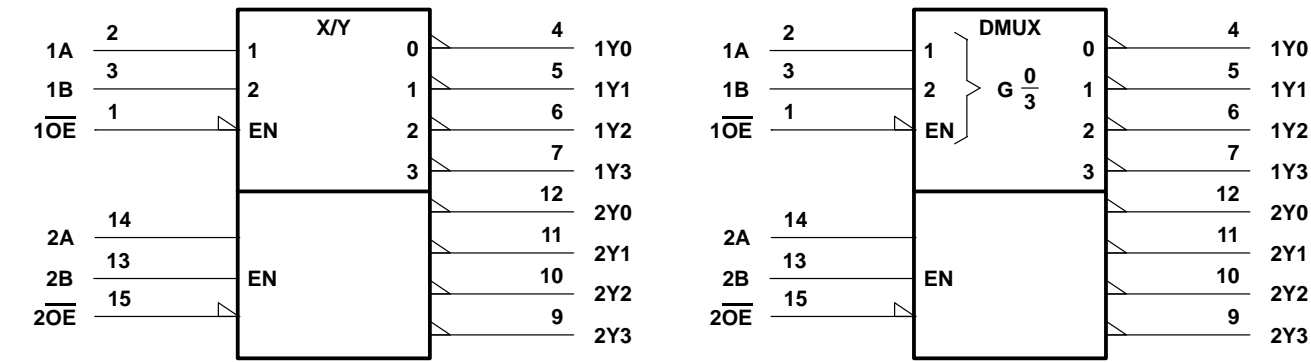
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
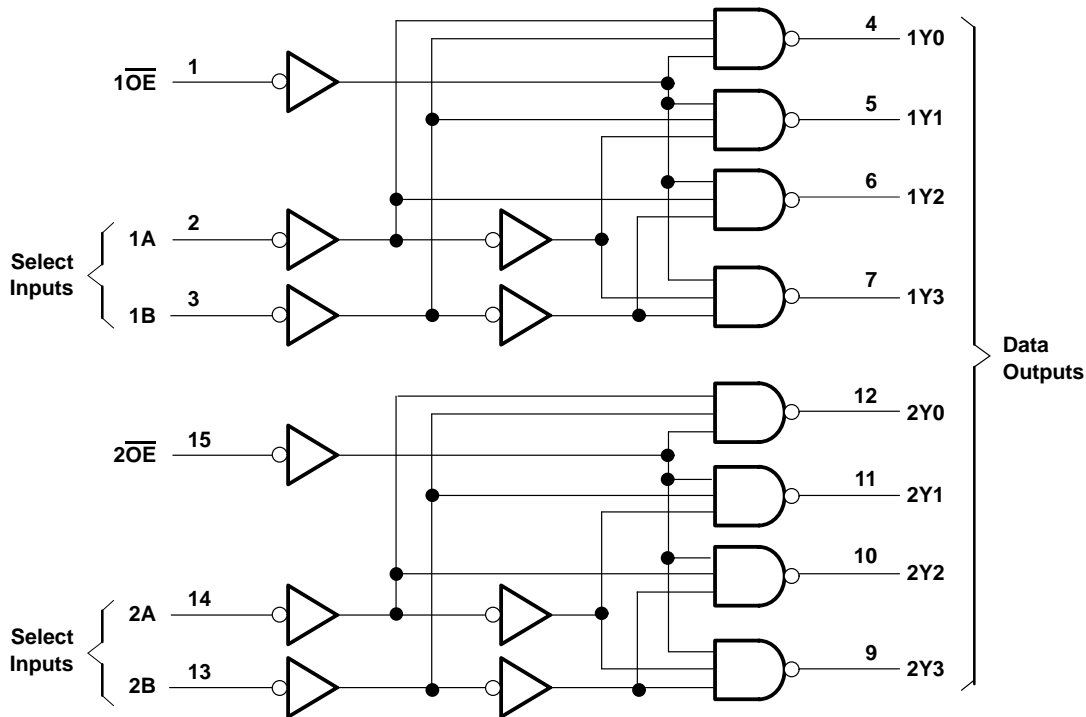
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package .... 113°C/W
  DB package .... 131°C/W
  PW package .... 149°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall time		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu A$		2.7 V to 3.6 V	V_{CC}–0.2			V
	$I_{OH} = -12\ mA$		2.7 V	2.2			
			3 V	2.4			
	$I_{OH} = -24\ mA$		3 V	2.2			
V_{OL}	$I_{OL} = 100\ \mu A$		2.7 V to 3.6 V			0.2	V
	$I_{OL} = 12\ mA$		2.7 V			0.4	
	$I_{OL} = 24\ mA$		3 V			0.55	
I_I	$V_I = 5.5\ V$ or GND		3.6 V			±5	μA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6 V			10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\ V$,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V				pF
C_o	$V_O = V_{CC}$ or GND		3.3 V				pF

† All typical values are at $V_{CC} = 3.3\ V$, $T_A = 25°C$.

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