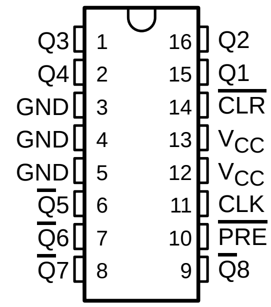
- **Replaces SN74AS305**
- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **TTL-Compatible Inputs and Outputs**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic Small-Outline (D) Package and Standard Plastic (N) 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The CDC305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. Preset ($\overline{PRE}$) and clear ($\overline{CLR}$) inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the clock (CLK) input.

The CDC305 has output and pulse-skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

The CDC305 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q4	$\overline{Q}$5–$\overline{Q}$8
L	H	X	L	H
H	L	X	H	L
L	L	X	L†	L†
H	H	L	Q_0	$\overline{Q}_0$
H	H	↑	$\overline{Q}_0$	Q_0

† This configuration does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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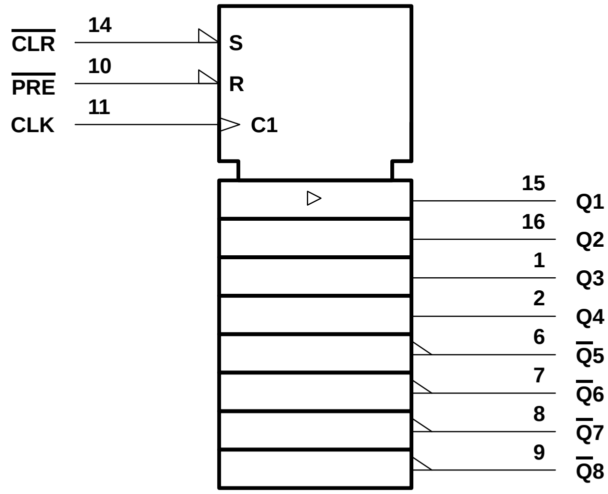
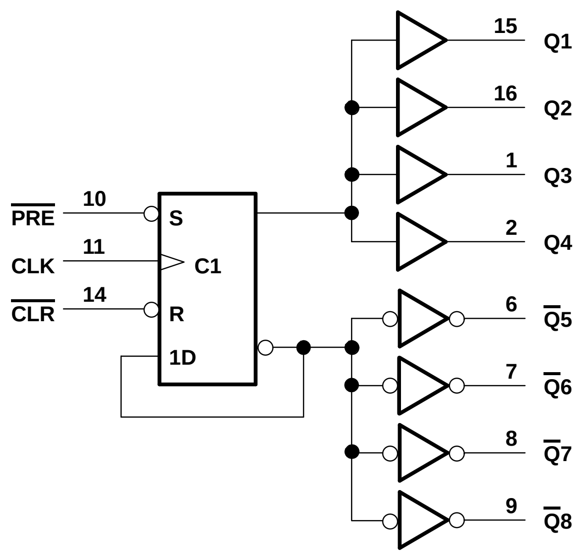
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . 7 V
Input voltage, V_I . . . . 7 V
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): D package . . . . 0.77 W
N package . . . . 1.2 W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 300 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = –24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–50		–150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 2		40	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

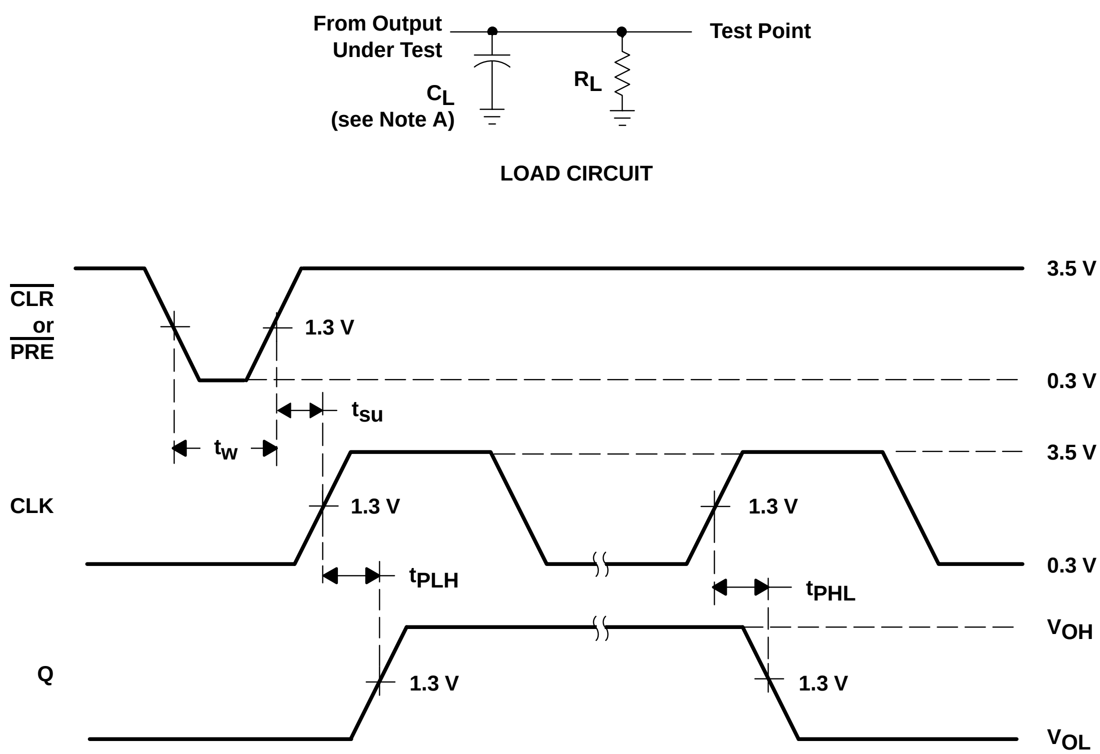
			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5		ns
		CLK high	4		
		CLK low	6		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}‡				80			MHz
t_{PLH}	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	2	6	9	ns
t_{PHL}				2	6	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	3	7	12	ns
t_{PHL}				3	7	12	
$t_{sk(o)}$	CLK	$\overline{Q}$	R_L = 500 Ω, C_L = 10 pF to 30 pF, See Figure 2			1	ns
		Q				1	
		Q1–$\overline{Q}$8				1.5	
$t_{sk(p)}$	CLK	Q1, $\overline{Q}$8	R_L = 500 Ω, C_L = 10 pF to 30 pF			1.5	ns
		Q2–$\overline{Q}$7				2	
t_r						4.5	ns
t_f						3.5	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ f_{max} minimum values are at C_L = 0 to 30 pF.

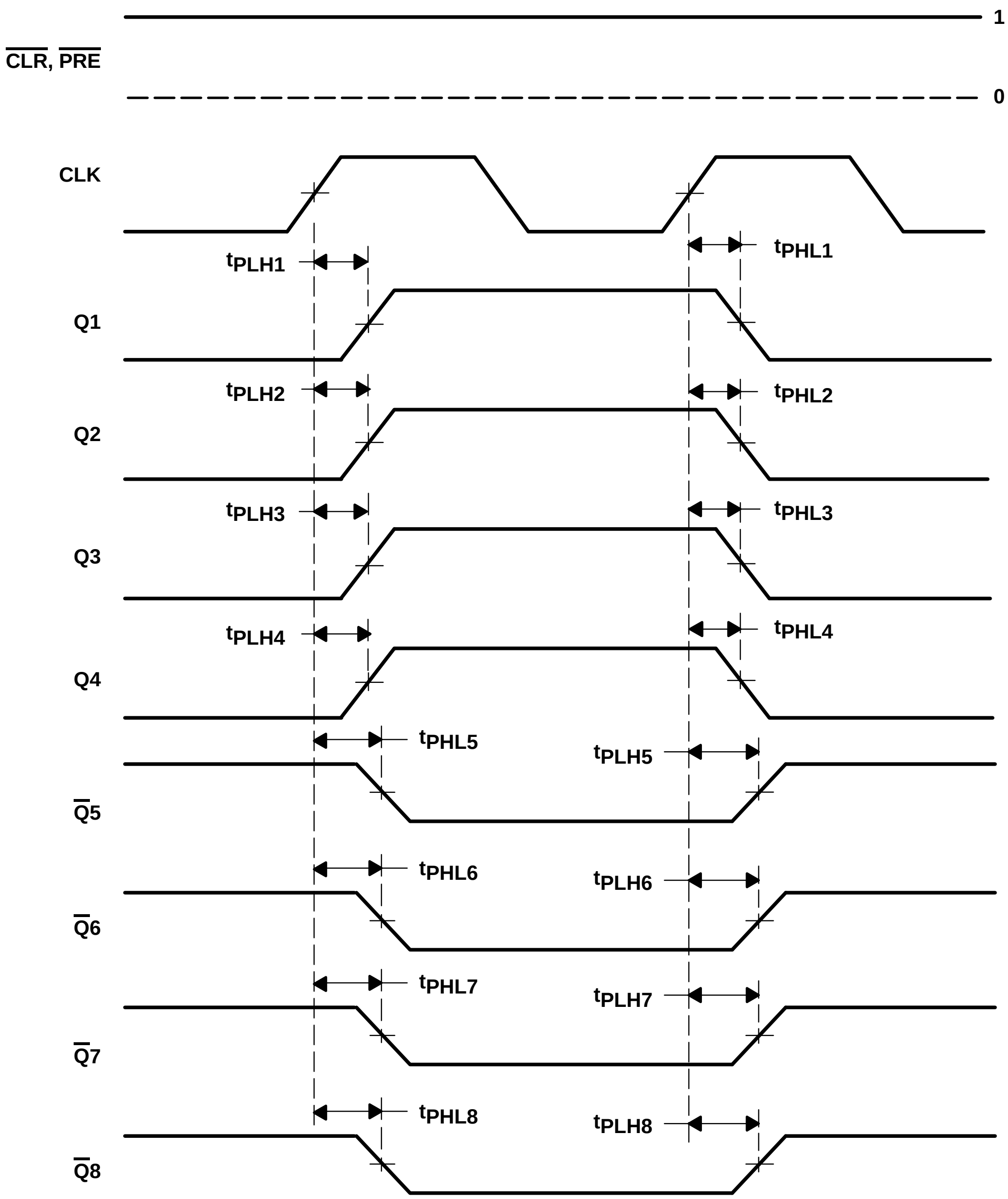
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $t_{sk(o)}$ CLK to Q are calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4)

B. $t_{sk(o)}$ CLK to $\overline{Q}$ are calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 5, 6, 7, 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 5, 6, 7, 8)

C. $t_{sk(o)}$ CLK to Q and $\overline{Q}$ are calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4), t_{PHLn} (n = 5, 6, 7, 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4), t_{PLHn} (n = 5, 6, 7, 8)

D. $t_{sk(p)}$ is calculated as the greater of | $t_{PLHn} - t_{PHLn}$ | (n = 1, 2, 3, . . . , 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(p)}$

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