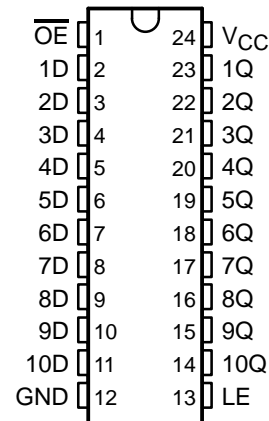


# SN74LVC841A 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE  
(TOP VIEW)



## description

This 10-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC841A is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC841A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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**TEXAS  
INSTRUMENTS**

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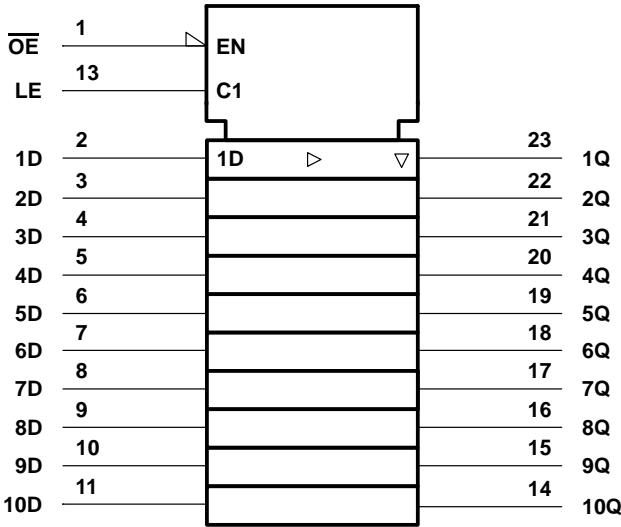
SN74LVC841A  
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FUNCTION TABLE

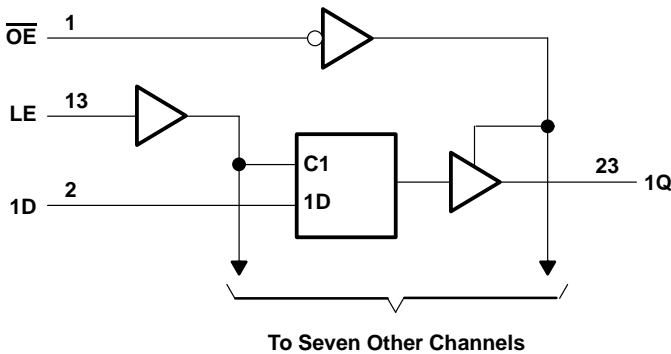
INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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## 10-BIT BUS-INTERFACE D-TYPE LATCH

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) (see Note 2)	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$ Supply voltage	Operating	2	3.6	V
	Data retention only	1.5		
$V_{IH}$ High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
$V_{IL}$ Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
$V_I$ Input voltage		0	5.5	V
$V_O$ Output voltage	High or low state	0	$V_{CC}$	V
	3 state	0	5.5	
$I_{OH}$ High-level output current	$V_{CC} = 2.7$ V		–12	mA
	$V_{CC} = 3$ V		–24	
$I_{OL}$ Low-level output current	$V_{CC} = 2.7$ V		12	mA
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
$T_A$ Operating free-air temperature		–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



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## 10-BIT BUS-INTERFACE D-TYPE LATCH

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = –100 µA	2.7 V to 3.6 V	V <sub>CC</sub> – 0.2			V
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I <sub>OH</sub> = –24 mA	3 V	2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	2.7 V to 3.6 V	0.2			V
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			
	I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V	±5			µA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	±10			µA
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V	±10			µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	10			µA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V‡		10			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7			pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This applies in the disabled state only.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	2.1		2.1		ns
t <sub>h</sub>	Hold time, data after LE↓	1		1		ns

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	2.4	6.7		7.5	ns
	LE		2.7	7.6		8.6	
t <sub>en</sub>	$\overline{\text{OE}}$	Q	1.3	7.2		8.5	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Q	1.9	5.9		6.6	ns
t <sub>sk(o)</sub> §				1			ns

§ Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

**operating characteristics, V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per latch	C <sub>L</sub> = 0, f = 10 MHz	25	pF
	Outputs enabled Outputs disabled		6	



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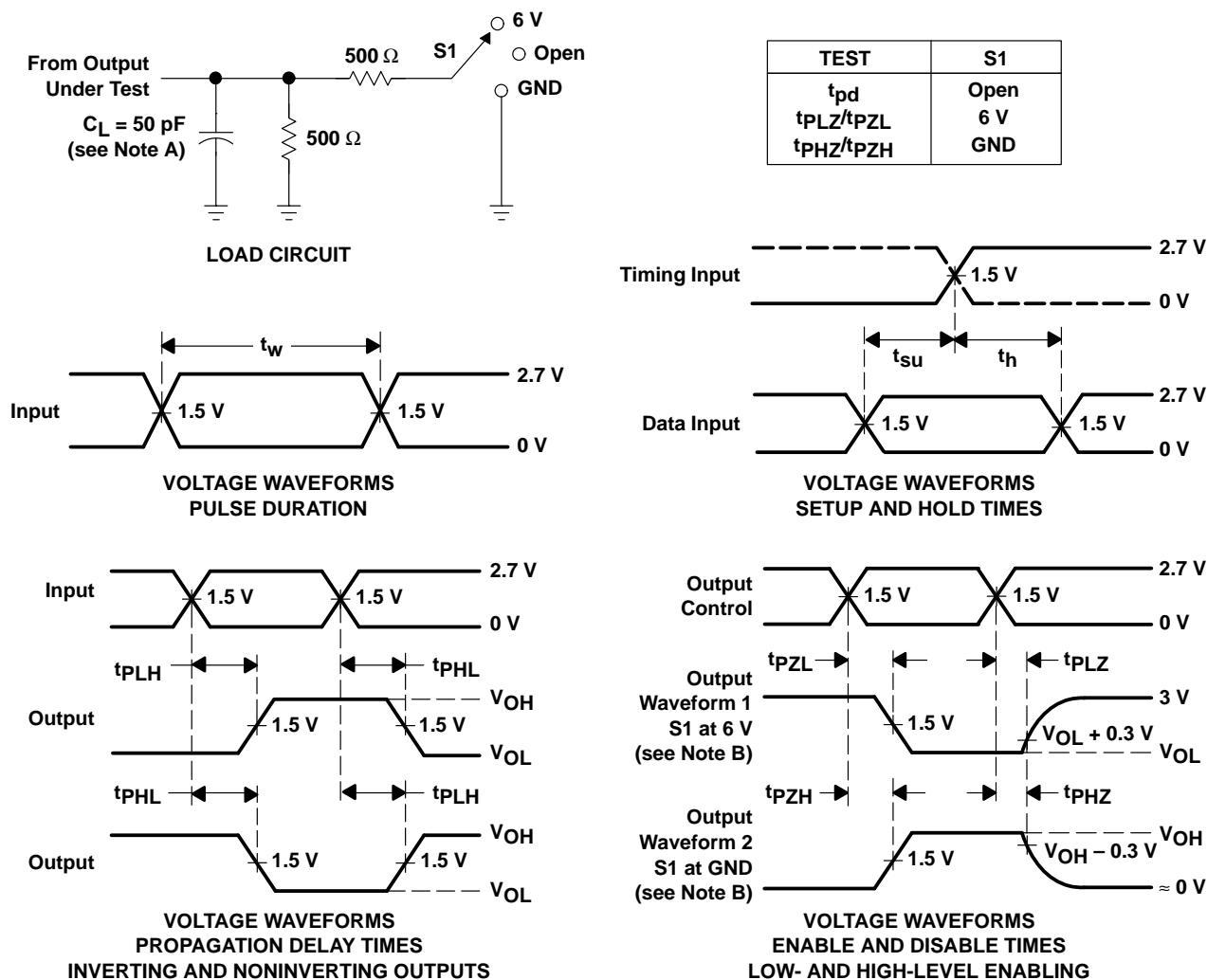
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#### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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