SN74LVC541A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS298E - JANUARY 1993 - REVISED JUNE 1997

20 🛛 V_{CC}

19 OE2

18 **1** Y1

17 Y2

16 Y3

15 **1** Y4

14 **1** Y5

13 **1** Y6

12 Y7

11 **1** Y8

DB, DW, OR PW PACKAGE (TOP VIEW)

OE1

A1 **[**2

A2 🛙 3

A3 **1**4

A5 🛚 6

A6 🛛 7

A7 🛿 8

A8 🛛 9

GND 10

5

A4 [

- *EPIC* [™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC541A is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC541A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE							
	INPUTS	OUTPUT					
OE1	OE2	Α	Y				
L	L	L	L				
L	L	Н	Н				
н	Х	Х	Z				
Х	Н	Х	Z				



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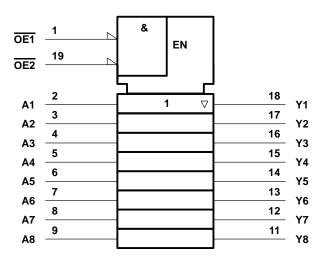


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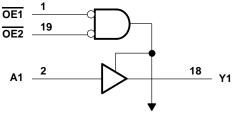
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state, V _O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_{f O}$	
(see Notes 1 and 2)	–0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$ (see Note 2)	
Continuous current through V _{CC} or GND	
Package thermal impedance, θ_{JA} (see Note 3): DB package	
DW package	
PW package	
Storage temperature range, T _{stg}	

\$ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The value of V_{CC} is provided in the recommended operating conditions table.

3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vaa	Sumhundhaga	Operating	2	3.6	V	
Vcc S	Supply voltage	Data retention only	1.5		v	
VIH	High-level input voltage	$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		V	
VIL	Low-level input voltage	$V_{CC} = 2.7 V \text{ to } 3.6 V$		0.8	V	
VI	Input voltage		0	5.5	V	
Vo	Output voltage	High or low state	0	VCC	V	
V0		3 state	0	5.5	v	
lau	High-level output current	$V_{CC} = 2.7 V$		-12	mA	
IOH I	High-level output current	$V_{CC} = 3 V$		-24	4	
IOL		$V_{CC} = 2.7 V$	12		~^^	
	Low-level output current	$V_{CC} = 3 V$		24	mA	
ТĄ	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP†	MAX	UNIT	
	I _{OH} = -100 μA		2.7 V to 3.6 V	V _{CC} -0.2				
Maria	I _{OH} = -12 mA		2.7 V	2.2			V	
VOH			3 V	2.4				
	I _{OH} = -24 mA	I _{OH} = -24 mA		2.2				
	I _{OL} = 100 μA		2.7 V to 3.6 V			0.2		
VOL	I _{OL} = 12 mA		2.7 V			0.4	V	
	I _{OL} = 24 mA		3 V			0.55		
lլ	V _I = 0 to 5.5 V		3.6 V			±5	μA	
l _{off}	$V_{I} \text{ or } V_{O} = 5.5 \text{ V}$		0			±10	μA	
I _{OZ}	V _O = 0 to 5.5 V		3.6 V			±10	μA	
	$V_{I} = V_{CC}$ or GND	I ^O = 0	3.6 V			10	A	
Icc	$3.6 V \le V_{I} \le 5.5 V^{\ddagger}$					10	μA	
ΔICC	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA	
Ci	$V_I = V_{CC}$ or GND		3.3 V		4		pF	
Co	$V_{O} = V_{CC} \text{ or } GND$		3.3 V		5.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. [‡] This applies in the disabled state only.



SN74LVC541A **OCTAL BUFFER/DRIVER** WITH 3-STATE OUTPUTS

SCAS298E - JANUARY 1993 - REVISED JUNE 1997

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

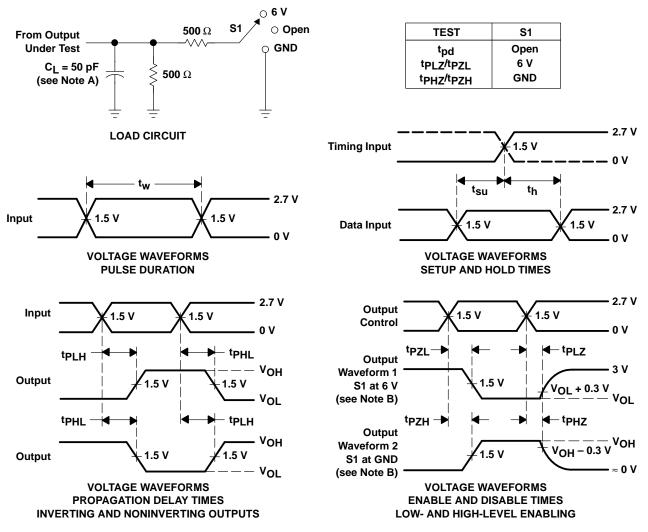
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
^t pd	А	Y	1.5	5.1		5.6	ns
t _{en}	OE	Y	1.5	7		7.5	ns
^t dis	OE	Y	1.5	7		7.7	ns
t _{sk(o)} †				1			ns

[†] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CO	ONDITIONS	TYP	UNIT
C _{pd}	Dower discipation conscitutes per huffer/driver	Outputs enabled	- C _L = 0,	f = 10 MHz	33	pF
	Power dissipation capacitance per buffer/driver	Outputs disabled			2	





PARAMETER MEASUREMENT INFORMATION

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.

 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tPZL and tPZH are the same as ten.
 - F. tpLz and tpHz are the same as tdis.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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