

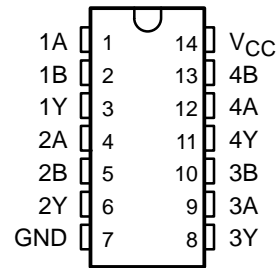
SN74LVC86A

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS288D – JANUARY 1993 – REVISED JANUARY 1997

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input exclusive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation. The SN74LVC86A performs the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC86A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

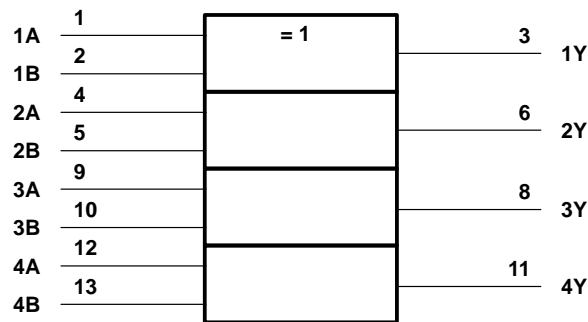
Copyright © 1997, Texas Instruments Incorporated

SN74LVC86A

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS288D – JANUARY 1993 – REVISED JANUARY 1997

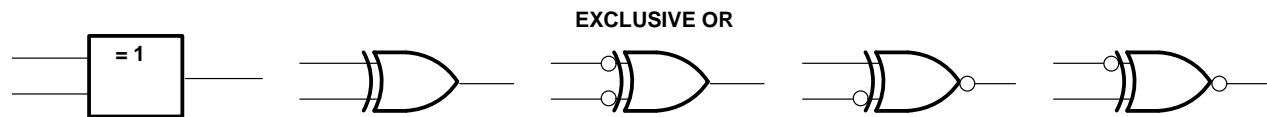
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

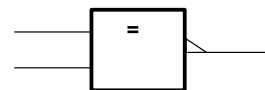
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



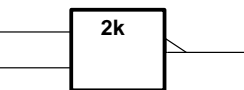
These five equivalent exclusive-OR symbols are valid for an SN74LVC86A gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



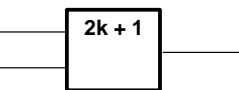
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

SN74LVC86A

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS288D – JANUARY 1993 – REVISED JANUARY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		–12	mA
		$V_{CC} = 3$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	9	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74LVC86A

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS288D – JANUARY 1993 – REVISED JANUARY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	2.7 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	2.7 V to 3.6 V	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	4.6	5.6		ns
t _{sk(o)} †			1				ns

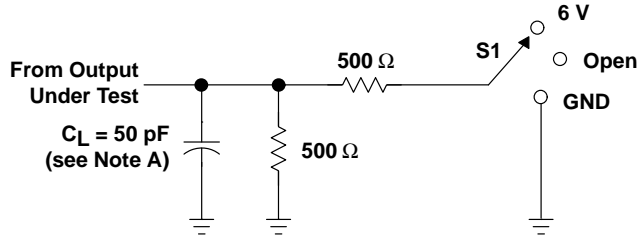
† Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 10 MHz	8.5	pF

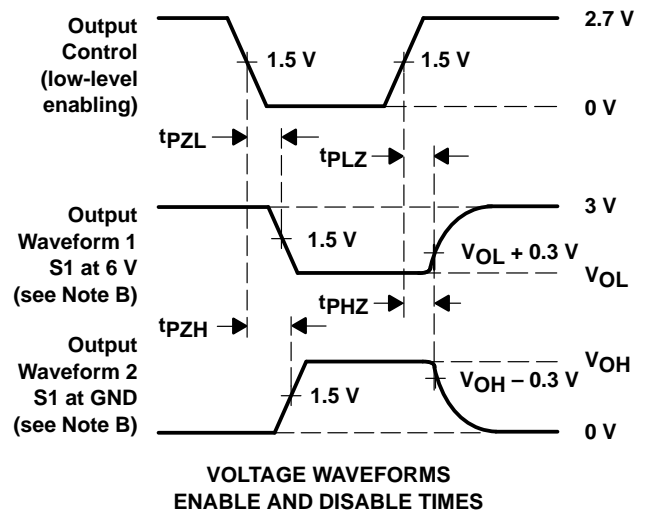
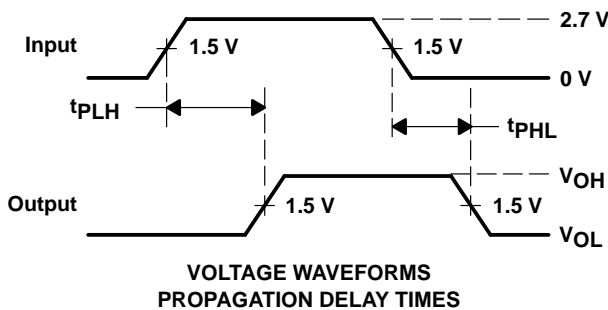
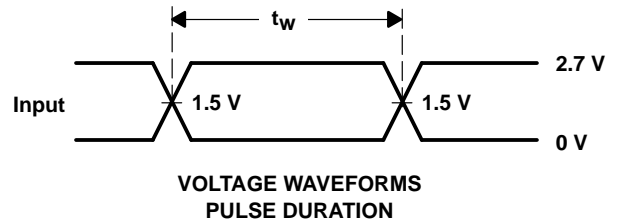
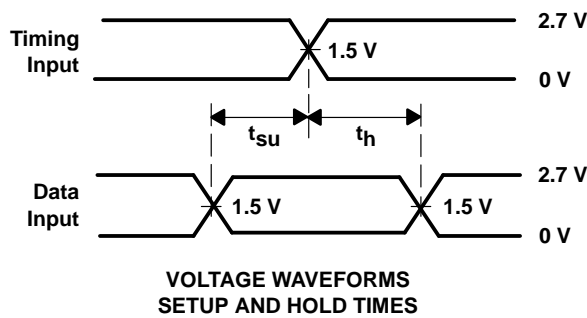


PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.